Modeling the Overshooting Effect for CMOS Inverter Delay Analysis in Nanometer Technologies

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***Abstract*—With the scaling of complementary metal–oxide–semiconductor (CMOS) technology into the nanometer regime, the overshooting effect due to the input-to-output coupling capacitance has more significant influence on CMOS gate analysis, especially on CMOS gate static timing analysis. In this paper, the overshooting effect is modeled for CMOS inverter delay analysis in nanometer technologies. The results produced by the proposed model are close to simulation program with integrated circuit emphasis (SPICE). Moreover, the influence of the overshooting effect on CMOS inverter analysis is discussed. An analytical model is presented to calculate the CMOS inverter delay time based on the proposed overshooting effect model, which is verified to be in good agreement with SPICE results. Furthermore, the proposed model is used to improve the accuracy of the switch-resistor model for approximating the inverter output waveform.**

***Index Terms*—CMOS inverter, gate delay, nanometer technology, overshooting time, switch-resistor model, timing analysis.**

I. Introduction

DUE TO THE input-to-output coupling capacitance, the complementary metal–oxide–semiconductor (CMOS) gate output voltage will be beyond the power supply range at the beginning of the transition. That is known as the overshooting effect and the time during which the output voltage is out of the supply voltage range is defined as the overshooting time. For the CMOS gate using conventional long channel transistors, the overshooting effect is seldom of importance in digital circuits and is only of major importance in analog circuits [1]. Traditional gate delay models [2]–[6] associate a constant delay to an output-load related characteristic of its size and input signal transition time without taking into account the influence of the input-to-output coupling capacitance. Similarly, the CMOS gate switch-resistor model in [7] and the short-circuit power estimation model in [8] also ignored the influence of overshooting effect.

With the scalingof CMOS technology into submicronmeter features sizes, the overshooting effect becomes significant and thus begin to be considered in CMOS gate analysis. In [9]–[16], the nonlinearity induced by the input-to-output coupling capacitance is taken into account for gate delay models. In [17], [18], the power consumption estimation models of CMOS buffers were given accounting for the influence of the input-to-output coupling capacitance in submicronmeter technologies. Since the overshooting time becomes one of important parameters for CMOS gate timing analysis or power consumption estimation, several empirical models have been proposed to estimate overshooting time. In [12], an expression was derived to compute the CMOS gate delay time while the step input delay time was required. In [18], an empirical model was proposed to estimate CMOS gate power consumption. However, these models are still not accurate enough in various conditions.

As CMOS technology enters nanometer regime, the overshooting effect due to the input-to-output coupling capacitance becomes more significant and cannot be neglected anymore because it has much influence on CMOS gate analysis including CMOS circuit timing prediction, power estimation, and output waveform approximation. However, there has been still few researches to focus on the overshooting time estimation in nanometer technologies. It has been customarily assumed as constant values or zero. Therefore, it is necessary to develop an accurate model of overshooting time suitable for CMOS gate analysis. At the same time, it is also required to improve conventional CMOS gate delay models when the increasing influence of the input-to-output coupling capacitance is considered.

In this paper, the overshooting effect due to the input-to-output coupling capacitance is modeled for the CMOS

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inverter delay analysis in nanometer technologies. By using the proposed overshooting time model, an analytical delay model is presented for CMOS inverters, and an improved switch-resistor model is given to approximate the inverter output waveform. The major contributions of this paper are as follows.

1) The overshooting effect of CMOS inverter due to input-to-output coupling capacitance is demonstrated to have much influence on CMOS gate timing analysis.
2) The overshooting effect is modeled for the CMOS inverter analysis in nanometer technologies. The overshooting time predicted by the proposed model is verified with 32 nm predictive technology model (PTM) [21], [22] to be close to simulation program with integrated circuit emphasis (SPICE). Since the linear approximation for MOS transistor drain current is used, the proposed model can eliminate numerical iteration, and thus results in short calculation time.
3) The proposed model is verified to be applicable to various device models such as 32 nm PTM high-k/metal-gate model [21], [22].
4) An analytical model is proposed to calculate the CMOS inverter delay time based on the overshooting effect model, and is verified to be in good agreement with SPICE results.
5) The practical application of the proposed overshooting effect model is shown to improve the accuracy of the switch-resistor model. The simulation results show that the switch-resistor model using the proposed overshooting time model can accurately predict the CMOS inverter output waveform.

The rest of this paper is organized as follows. The problem formulation is described in Section II. The proposed analytical model of overshooting time is given in Section III. CMOS inverter delay model considering the overshooting effect is shown in Section IV, and the switch-resistor model considering the influence of the coupling capacitance is given in Section V. This paper is concluded in Section VI.

II. Preliminaries

Fig. 1 shows a CMOS inverter with capacitive load C_L, where the input-to-output coupling capacitance C_M is considered. Fig. 2 shows the output voltage V_{out} of CMOS inverter for a falling input V_{in} using CMOS 32 nm PTM model [21], [22]. t_{50} is the time for the gate output voltage from the initial point to 50% V_{DD} point and t_{50} consists of the following two parts.

1) Overshooting time t_{ov}, which is caused by the input-to-output coupling capacitance as shown in Fig. 2.
2) Gate output waveform rise time t_r from $t = t_{\text{ov}}$ to 50% V_{DD} point.

We thus have

$$t_{50} = t_{\text{ov}} + t_r. \tag{1}$$

The gate propagation delay t_D is defined as the time interval from $V_{\text{in}} = V_{DD}/2$ to $V_{\text{out}} = V_{DD}/2$. From Fig. 2, we can obtain

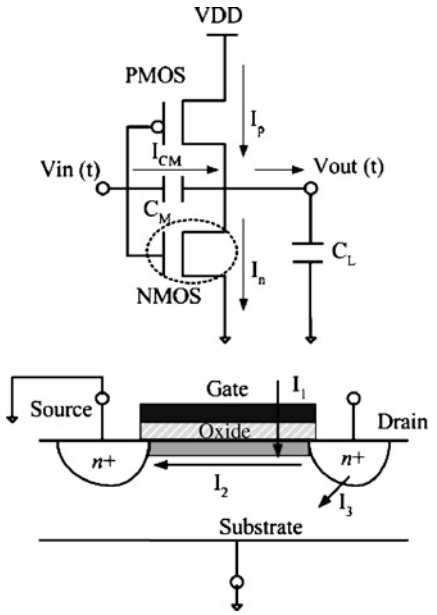

Fig. 1. CMOS inverter model and transistor leakage currents.

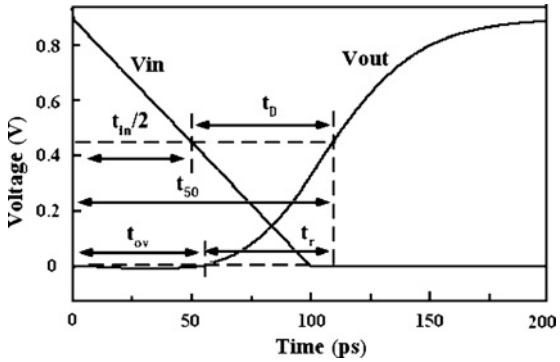

Fig. 2. Output voltage of CMOS inverter for a falling input.

the gate delay as

$$t_D = t_{50} - \frac{t_{\text{in}}}{2}. \tag{2}$$

It is known that CMOS gate output waveform t_{50} in nanometer technologies consists of two main parts. One is the output rise time t_r. The other is the overshooting time t_{ov} which is generally ignored in traditional research. The delay time t_D is thus expressed as

$$t_D = t_{\text{ov}} + t_r - \frac{t_{\text{in}}}{2}. \tag{3}$$

Fig. 3 shows the rise time t_r and the overshooting time t_{ov} for various inverter sizes using the same 32 nm process model. The negative channel metal–oxide–semiconductor (NMOS) width W_n varies from 80 nm to 800 nm with $W_p = 2W_n$. Both positive channel metal–oxide–semiconductor (PMOS) and NMOS transistor length L is 40 nm. The capacitive load C_L is equal to 0.01 pF, and the input signal transition time t_{in} is 50 ps. From Fig. 3, it can be seen that the rise time decreases greatly as the inverter width increases. The overshooting time t_{ov}, in contrast, changes little with the increase of inverter size.

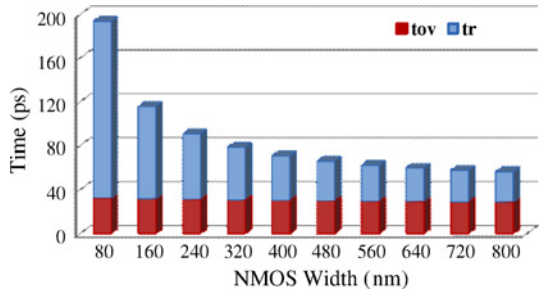

Fig. 3. Gate output waveform rise time t_r and overshooting time t_{ov} with various inverter sizes.

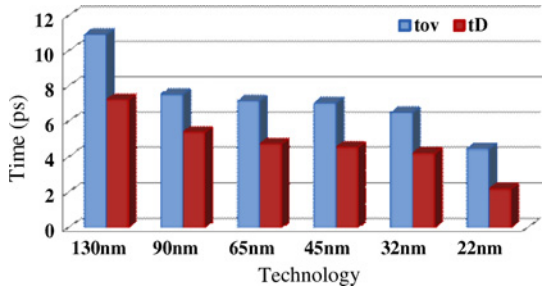

Fig. 4. Gate output waveform rise time t_r and overshooting time t_{ov} with various technologies.

Fig. 4 shows the delay time t_D and the overshooting time t_{ov} for various process technologies from 130 nm to 22 nm with typical supply voltages [23]. The transistor length L is the minimum feature size. The widths of all PMOS transistors W_p are ten times of L while W_p is two times of W_n. The load capacitance C_L is 0.01 pF. The input transition time t_{in} is also 50 ps. From Fig. 4, it is clearly shown that both times t_D and t_{ov} decrease with the scaling of the process technologies. However, the ratio of t_{ov}/t_D increases from 151% at 130 nm process to 202% at 22 nm process.

Therefore, it is inferred from the simulation results in Figs. 3 and 4 that the overshooting time t_{ov} becomes one of the most dominant parts of the output waveform of the CMOS inverter as the process technologies enter nanometer regime. Moreover, the overshooting time t_{ov} contributes much more to t_{50} when the inverter size increases. Consequently, the overshooting effect has more significant influence on CMOS inverter analysis, especially on static timing analysis in nanometer technology.

Currently, the use of delay models for performance cell-based delay calculation has become an industry standard in practical delay calculation tools. As cells are connected together by interconnect wires, the delay time of CMOS circuits between the input signal to output signal is just the sum of the delay time of each cell. Since the overshooting time t_{ov} is one of the most important part of the delay time, the total overshooting time of each cell is also accumulated in the delay time estimation.

To illustrate this, a chain of five inverters is used to observe the output waveform of each inverter as shown in Fig. 5. It can be seen that the overshooting time of the first gate propagates from stage to stage before it arrives the last one. The time when the output voltage V_{out5} begins to fall from V_{DD} to ground is

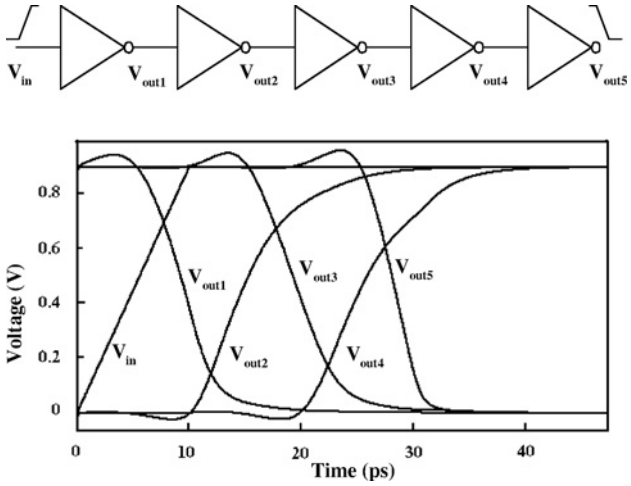

Fig. 5. Simulation results of the chain of inverters with 32 nm PTM model.

almost equal to the total overshooting time of all inverters. In Fig. 5, the delay time t_D of the inverter chain is 23.4 ps, while the overshooting time t_{ov} of all inverters is 25.32 ps which is larger than the delay time of the inverter chain.

It is clearly shown that the overshooting time is one of dominated parts in the inverter delay time estimation. Therefore, it is necessary to develop an accurate model for overshooting effect for the CMOS inverter analysis in nanometer technologies.

III. Modeling the Overshooting Effect

The differential equation for the CMOS inverter of Fig. 1 loaded by a coupling capacitance C_M can be described as

$$C_L \frac{dV_{out}}{dt} = I_p - I_n + C_M \frac{d(V_{in} - V_{out})}{dt} \tag{4}$$

where C_L is the output capacitive load including the inverter diffusion capacitance, the interconnect wire capacitance and the load gate input capacitance. Also, V_{out} and V_{in} are the gate output and input voltages, respectively. I_p and I_n are the PMOS and NMOS transistor currents, respectively. Here, the differential equation is solved only for the falling input ramp. Similar expressions can be derived for the rising input ramp. The input voltage for the falling input ramp is expressed as

$$V_{in} = \begin{cases} V_{DD} & : \quad t \le 0 \\ \left(1 - \frac{t}{t_{in}}\right) V_{DD} & : \quad 0 < t \le t_{in} \\ 0 & : \quad t > t_{in} \end{cases} \tag{5}$$

where t_{in} is the input falling time. The value of C_M in input high state consists of the side-wall capacitance of both transistors drain and the gate to drain overlap capacitance of NMOS transistor in the linear region [18]

$$C_M = C_{ox}\left(\frac{W_{n\,eff} L_{n\,eff}}{2} + X_{Dp} W_{p\,eff} + X_{Dn} W_{n\,eff}\right) \tag{6}$$

where $W_{p\,eff}$ and $W_{n\,eff}$ are PMOS and NMOS effective channel widths, respectively, while $L_{n\,eff}$ is the NMOS effective channel length. Also, X_{Dp} and X_{Dn} are the gate-drain

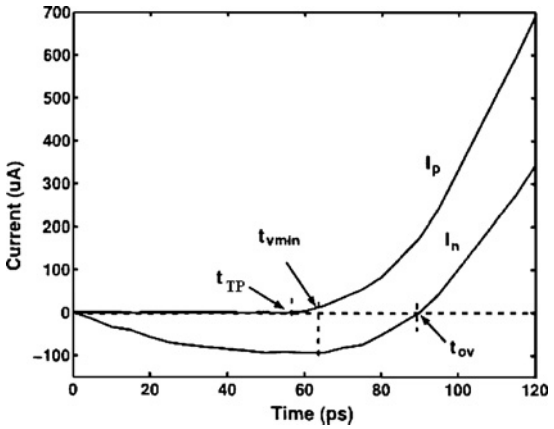

Fig. 6. PMOS and NMOS transistor drain currents I_p and I_n during the overlapping period.

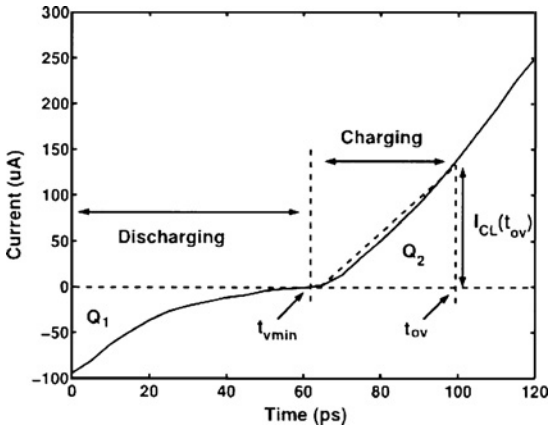

Fig. 7. Approximation of the current I_{C_L} during $t_{\rm ov}$.

underdiffusion for PMOS and NMOS transistors, respectively. $C_{\rm ox}$ is the gate-oxide capacitance per unit area.

Leakage current in deep-submicrometer regimes is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced [24]. Fig. 1 shows an NMOS transistor considering leakage currents, which include the oxide tunneling current I_1, the subthreshold leakage I_2, the reverse-bias pn junction leakage I_3, and so on. Commonly, the leakage components have very important influence for estimation and reduction of leakage power, especially for low-power applications. For the overshooting effect analysis, however, its influence is very small and can be ignored in the proposed method because the current components in (4) are much larger than the leakage currents.

In the proposed model, we firstly define two time points t_{TP} and $t_{v\,\rm min}$. As shown in Fig. 6, t_{TP} is the time when the PMOS transistor is on and $t_{TP} = (|V_{TP}|/V_{DD})t_{\rm in}$, where V_{TP} is the threshold voltage of PMOS transistor. Also, $t_{v\,\rm min}$ is the time when the output voltage is at its minimum. Then the overshooting period can be divided into following two parts.

1) $t_{TP} \geq t > 0$: PMOS transistor is off. The voltage of the capacitance C_L decreases from zero due to a partial discharge through coupling capacitance.
2) $t_{\rm ov} \geq t > t_{TP}$: PMOS transistor begins to conduct and the PMOS current I_p charges the load capacitance C_L. Then the voltage of the load capacitance increases. Once the output voltage goes up to zero, the NMOS current I_n becomes positive.

A. Proposed Model for $t_{\rm ov}$

At the time $t = t_{\rm ov}$, the charge of C_L is zero and the gate output waveform rises from zero. Therefore, we have

$$Q_L = Q_2 - Q_1 = 0 \tag{7}$$

where Q_1 is the charge flowing out of C_L, and Q_2 is the charge flowing into C_L during the overshooting time.

We rearrange (4) as

$$I_{C_L} = I_p - I_n + I_{CM} \tag{8}$$

where I_{C_L} is the load current and I_{CM} is the current flowing through the coupling capacitance C_M. When $t < t_{TP}$, $I_{C_L} = I_{CM} - I_n$. When $t = t_{TP}$, the PMOS transistor turns on. Then $I_{C_L} = I_p - I_n + I_{CM}$. Fig. 7 shows the load current I_{C_L} during the overlapping period. As shown in Fig. 7, the load current I_{C_L} can be assumed as linear during the charge time $t > t_{v\,\rm min}$, that is verified to be valid by SPICE simulations for various simulation conditions. Therefore, we can derive a simple expression for Q_2 as

$$Q_2 = \int_{t_{v\,\rm min}}^{t_{\rm ov}} I_{C_L}(t)dt \approx \frac{I_{C_L}(t_{\rm ov})}{2}[t_{\rm ov} - t_{v\,\rm min}] \tag{9}$$

where $I_{C_L}(t_{\rm ov})$ is the output load current when $t = t_{\rm ov}$. Since $Q_1 = Q_2$, we obtain

$$t_{\rm ov} = \frac{2Q_1}{I_{C_L}(t_{\rm ov})} + t_{v\,\rm min} \tag{10}$$

where the second term $t_{v\,\rm min}$ corresponds to the discharge time and the first term $2Q_1/I_{C_L}(t_{\rm ov})$ corresponds to the charge time.

When $t = t_{\rm ov}$, the drain current I_n should be zero because the drain-source voltage V_{DS} of NMOS transistor is zero. Also, due to $dV_{\rm in}/dt \gg dV_{\rm out}/dt$ during overshooting period, $I_{C_L}(t_{\rm ov})$ can be expressed as

$$I_{C_L}(t_{\rm ov}) = C_M\frac{dV_{\rm in}}{dt} + I_p(t_{\rm ov}) \tag{11}$$

where $I_p(t_{\rm ov})$ is the PMOS transistor current when $t = t_{\rm ov}$.

From (10) and (11), it is seen that the overshooting time $t_{\rm ov}$ is determined by Q_1, $t_{v\,\rm min}$ and $I_p(t_{\rm ov})$. In the following, we will show the detailed description of these three terms.

When $t \leq t_{TP}$, the PMOS transistor is cut off. Since $V_{DS} \ll V_{GS}$, the NMOS transistor drain current can be simply expressed as [1]

$$I_n \approx K'\frac{W}{L}(V_{GS} - V_{TN})V_{DS} \tag{12}$$

where K' is the transconductance parameter, V_{GS} is the gate-to-source voltage and V_{TN} is the NMOS transistor threshold voltage. Therefore, we have the expression

$$(C_L + C_M)\frac{dV_{\rm out}}{dt} + \beta_n(V_{GS} - V_{TN})V_{\rm out} = C_M\frac{dV_{\rm in}}{dt} \tag{13}$$

where $\beta_n = K'W/L$. When $t_{TP} < t < t_{v\,\min}$, the PMOS transistor is on and the expression for the output voltage is more complicated. It is also inferred from Figs. 6 and 7 that the output voltage V_{out} at $t_{v\,\min}$ is close to the one at t_{TP} because the load currents I_{C_L} at the two time points are almost zero. The reason can be expressed as follows. When $t < t_{TP}$, the current flowing out of the capacitive load begins to decrease to zero because of the NMOS drain current. Then from the time $t = t_{TP}$, the PMOS drain current starts to increase significantly, and the load current becomes zero in very short time. The solution of the differential equation when $t = t_{TP}$ is given as

$$V_{\text{out}}(t_{TP}) = \frac{C_M \frac{dV_{\text{in}}}{dt}}{\beta_n(V_{DD}-|V_{TP}|-V_{TN})}\left[1-e^{-\frac{\beta_n(V_{DD}-|V_{TP}|-V_{TN})}{C_L+C_M}\frac{t_{\text{in}}|V_{TP}|}{V_{DD}}}\right]. \tag{14}$$

Because of $V_{\text{out}}(t_{v\,\min}) \approx V_{\text{out}}(t_{TP})$, the charge Q_1 is obtained from the output voltage and expressed as

$$Q_1 \approx C_L V_{\text{out}}(t_{TP}). \tag{15}$$

When $t = t_{v\,\min}$, since $dV_{\text{out}}/dt = 0$, the current flowing into capacitance load is zero. Therefore, from (4) we can derive the PMOS transistor current when $t = t_{v\,\min}$ as

$$I_p(t_{v\,\min}) = I_n(t_{v\,\min}) - C_M\frac{dV_{\text{in}}}{dt} \tag{16}$$

where $I_n(t_{v\,\min})$ is the NMOS transistor current when $t = t_{v\,\min}$. Since the value of $V_{\text{out}}(t_{v\,\min})$ is close to $V_{\text{out}}(t_{TP})$, $I_n(t_{v\,\min}) \approx I_n(t_{TP})$. Then substituting (14) into (12), we obtain

$$I_n(t_{v\,\min}) \approx C_M\frac{dV_{\text{in}}}{dt}\left[1-e^{-\frac{\beta_n(V_{DD}-|V_{TP}|-V_{TN})}{C_L+C_M}\frac{|V_{TP}|}{V_{DD}}t_{\text{in}}}\right]. \tag{17}$$

The assumption in (17) is reasonable because its accuracy is determined mainly by the approximation for $V_{\text{out}}(t_{v\,\min})$.

As shown in Fig. 8, the α-power approximation is very close to SPICE simulation to predict the PMOS transistor current. Thus, the α-power metal–oxide–semiconductor field effect transistor (MOSFET) model [4] is used to calculate $t_{v\,\min}$, and is written as

$$I_p(t_{v\,\min}) = I_{D0}\left(\frac{|V_{GS}|-|V_{TP}|}{V_{DD}-|V_{TP}|}\right)^{\alpha} \tag{18}$$

where I_{D0} is the drain current in saturation at $V_{GS} = V_{DS} = V_{DD}$, α is the velocity saturation index and V_{GS} is a function of $t_{v\,\min}$. Note that although α-power MOSFET model was proposed for submicronmeter transistor, it is still helpful to model the transistor drain current in nanometer technologies, especially when the drain-source voltage is almost constant such as during the overshooting effect period. In this paper, α is assumed as 1.57 for 32 nm PTM model, which is verified by SPICE simulation results. Thus, we obtain the expression of $t_{v\,\min}$

$$t_{v\,\min} = t_{TP} + (t_{\text{in}} - t_{TP})\left[\frac{C_M V_{DD}}{I_{D0}t_{\text{in}}}e^{-\frac{\beta_n(V_{DD}-|V_{TP}|-V_{TN})}{C_L+C_M}\frac{|V_{TP}|}{V_{DD}}t_{\text{in}}}\right]^{\frac{1}{\alpha}}. \tag{19}$$

In (10), I_{C_L} is also determined by t_{ov}. Although the α-power MOSFET model or some other more accurate models can be used to obtain t_{ov}, the solution of such a nonlinear problem will result in complicated computation. To avoid numerical procedures, an initial value for t_{ov} is first solved by using a linear transistor drain current model, as shown in Fig. 9. Note that V_G is the PMOS gate voltage when $t = t_{\text{ov}}$ and the transistor current is described as

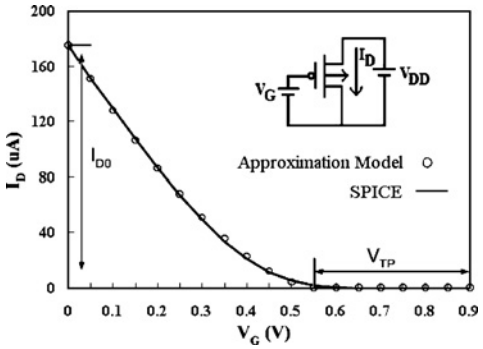

Fig. 8. α-power approximation for PMOS transistor drain current.

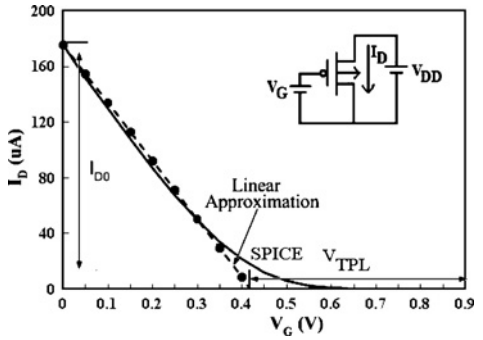

Fig. 9. Linear approximation for PMOS transistor drain current.

$$I_p = I_{D0}\left(\frac{|V_{GS}|-|V_{TPL}|}{V_{DD}-|V_{TPL}|}\right) \tag{20}$$

where V_{TPL} is the equivalent threshold voltages. The value is obtained by extending the line and intercept with x-axis. Also

$$|V_{GS}| = \frac{t_{\text{ov}}}{t_{\text{in}}}V_{DD}. \tag{21}$$

Through (10), (11), and (20), we can obtain

$$t_{\text{ov}} = \frac{2Q_1}{\frac{t_{\text{ov}}-t_{TPL}}{t_{\text{in}}-t_{TPL}}I_{D0} + C_M\frac{dV_{\text{in}}}{dt}} + t_{v\,\min} \tag{22}$$

where $t_{TPL} = \frac{|V_{TPL}|}{V_{DD}}t_{\text{in}}$. By solving (22), we then can derive the final expression for t_{ov} as

$$t_{\text{ov}} = t_{v\,\min} - t_\gamma + \sqrt{\frac{2Q_1}{I_{D0}}(t_{\text{in}}-t_{TPL}) + {t_\gamma}^2} \tag{23}$$

where

$$t_\gamma = \frac{1}{2}\left(t_{v\,\min} - t_{TPL} - C_M\frac{V_{DD}t_{\text{in}}}{t_{\text{in}}}\frac{t_{\text{in}}-t_{TPL}}{I_{D0}}\right). \tag{24}$$

Here, Q_1 and $t_{v\,\min}$ are obtained using (15) and (19).

Table I shows the calculation results for t_{ov} with (23). It is inferred that the model using linear assumption for PMOS drain current is still not very accurate to estimate the

TABLE I
COMPARISON OF THE TWO CALCULATION APPROACHES FOR t_{ov}

Input Signal (ps)	Overshooting Time (ps)			Error (%)	
	SPICE	(23)	Improved	(23)	Improved
20	16.38	14.9	16.15	13.90	1.40
100	57.64	54.68	58.36	5.13	1.25
200	101.6	101.31	101.38	0.29	0.22
300	141.5	147.5	140.5	4.24	0.70

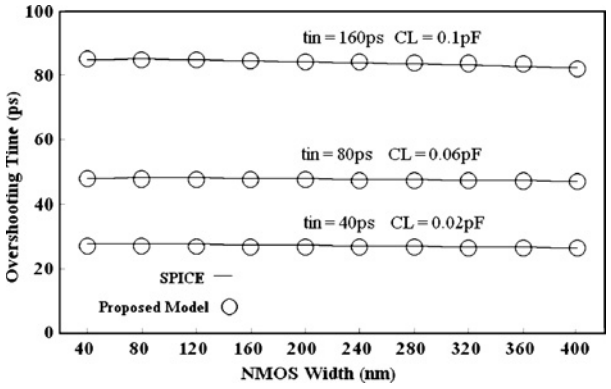

Fig. 10. Overshooting time t_{ov} of the proposed method and SPICE simulation for various gate drivability.

overshooting time. Therefore, another step is given to improve the accuracy. Substituting the initial t_{ov} of (23) into α-power MOSFET model, the new drain current I_p is solved. Then using (10) and (11), the new value for t_{ov} is finally obtained. It is clearly demonstrated from Table I that the error to predict t_{ov} is reduced significantly by using the improved method.

It is possible to improve the accuracy further by using iterative computation based on new t_{ov}. However, the calculation time will increase because of numerical procedures. Moreover, the proposed method using only two steps is accurate enough to calculate the overshooting time.

B. Simulation Results

We have applied the proposed method to the CMOS inverters to further verify its appropriateness with the same CMOS 32 nm PTM model. Note that the length of all NMOS and PMOS transistors are set to be $L_n = L_p = 40$ nm. And the ratio of PMOS width to NMOS width is $W_p/W_n = 2/1$.

Fig. 10 plots the results of overshooting time versus transistor widths which vary from 40 nm to 400 nm. Results show that the overshooting time t_{ov} decreases a little when the gate size increases. Moreover, it is seen that the presented model matches very well with SPICE simulations within 1.6% error for various simulation conditions.

Fig. 11 shows the results of the proposed model and SPICE simulation with respect to the various capacitive loads. The capacitive load varies from 0.02 pF to 0.2 pF. Simulation results show that the overshooting time t_{ov} increases a little against the capacitive load. The proposed model provides a good estimation of the overshooting time for small and large capacitive loads within 3.01% error.

Fig. 12 compares the overshooting time of the proposed method, SPICE simulation and the model in [18] with respect

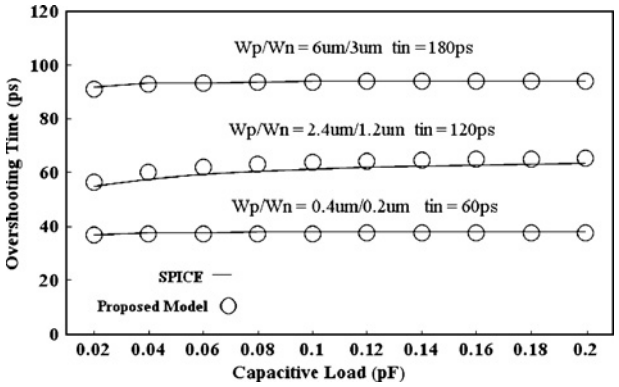

Fig. 11. Overshooting time t_{ov} of the proposed model and SPICE simulation for various capacitive loads.

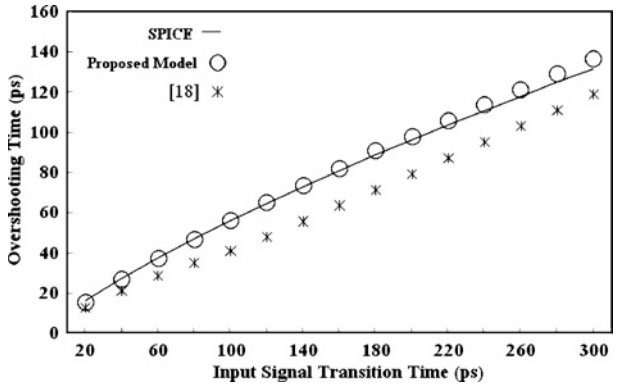

Fig. 12. Overshooting time t_{ov} of the proposed model and SPICE simulation for various input signal transition times.

to various input signal transition times. Note that the model was proposed in [18] for CMOS gate power estimation, and was also used to predict CMOS gate delay time in [16]. In Fig. 12, the input signal transition time ranges from 20 ps to 300 ps. Also the width of NMOS transistor W_n is 80 nm while the capacitive load is 0.01 pF. It can be observed that the presented analytical model for the evaluation of the overshooting time gives results close to those derived from SPICE simulations with 2.06% average error. Moreover, the prediction result of the model in [18] is not accurate compared with SPICE simulation with 19.72% average error.

From the simulation results in Figs. 10–12, it is clearly demonstrated that the proposed model is accurate for predicting the overshooting time t_{ov} in various conditions.

C. High-k/Metal-Gate Model

Since the gate oxide leakage current is increasing with decreasing SiO_2 thickness, its scaling is becoming exceedingly difficult. With further scaling, the high-k gate dielectrics and metal gate electrodes will be required for high-performance and low-power CMOS applications. Much work has been done for high-k/metal-gate transistors in [25], [26] recently. In this paper the proposed overshooting model is also applied to the inverter constructed with high-k/metal-gate transistor, where the 32 nm PTM high-k/metal-gate models for high-performance applications (PTM HP) and for low-power ap-

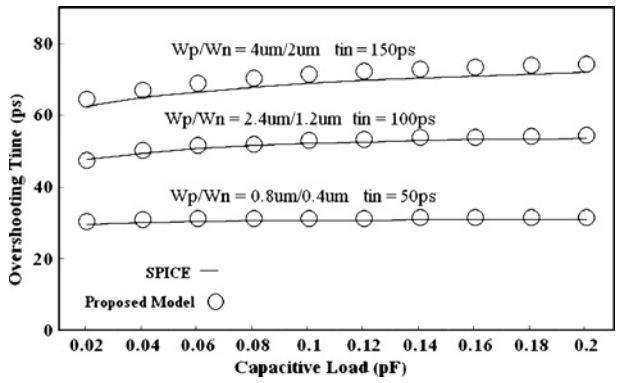

Fig. 13. Overshooting time t_{ov} of the proposed model and SPICE simulation for various capacitive loads with 32 nm PTM HP model.

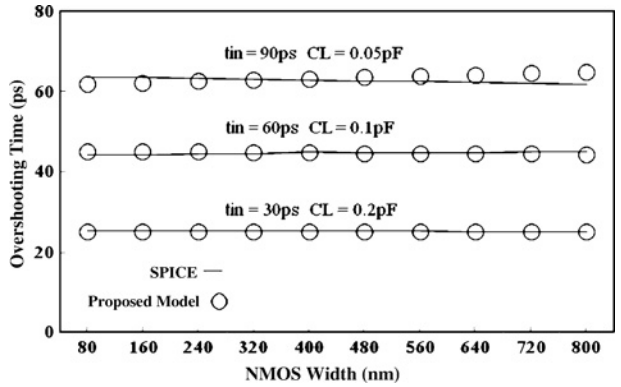

Fig. 14. Overshooting time t_{ov} of the proposed method and SPICE simulation for various gate drivability with 32 nm PTM LP model.

plications (PTM LP) [20], [21] are utilized in the SPICE simulation.

Fig. 13 shows the results of the proposed model and SPICE simulation with respect to the various capacitive loads, where 32 nm PTM HP model is used. The capacitive load varies from 0.02 pF to 0.2 pF. Simulation results show that the proposed model provides a good estimation of the overshooting time for various capacitive loads within 3.31% error.

Fig. 14 plots the results of overshooting time versus transistor widths which vary from 80 nm to 800 m with 32 nm PTM LP model. Results show that the proposed model reproduces the overshooting time accurately compared with SPICE simulations with 1.17% average error.

Figs. 13 and 14 demonstrate that the proposed model is applicable to predict the overshooting time of CMOS inverters for various device models such as the high-k/metal-gate model.

IV. CMOS Inverter Delay Analysis

In this section, the CMOS inverter delay analysis in nanometer technologies is discussed with considering overshooting effect because the delay time is one of the most important parameters for very-large-scale integration (VLSI) circuit performance.

As shown in (3), the delay time t_D in nanometer technologies can be obtained if the overshooting time t_{ov}, the rise time t_r and the input signal transition time t_{in} are known.

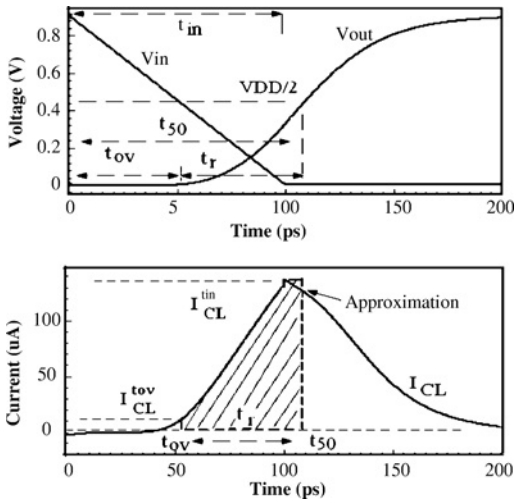

Fig. 15. Linear approximation for the current through capacitive load C_L to delay analysis.

Generally, the transition time t_{in} is given in delay calculation. In previous section, we have proposed an analytical model for the overshooting time t_{ov}. In the following, we will obtain the analytical expression of the rise time t_r.

A. Delay Model

Fig. 15 shows the output voltage and output current through capacitive load C_L for CMOS inverter in Fig. 1. It is seen that the output currents I_{CL} can be approximated linearly in order to simplify the analysis. Since the area with fill in Fig. 15 is just the total charges stored in capacitor C_L, we can obtain

$$\frac{I_{CL}^{t_{ov}} + I_{CL}^{t_{in}}}{2}(t_{in} - t_{ov}) + I_{CL}^{t_{in}}[t_r - (t_{in} - t_{ov})] = \frac{V_{DD}}{2}C_L. \quad (25)$$

Therefore, we can derive the expression for t_r as

$$t_r = \frac{V_{DD}C_L + (I_{CL}^{t_{in}} - I_{CL}^{t_{ov}})(t_{in} - t_{ov})}{2I_{CL}^{t_{in}}} \quad (26)$$

where $I_{CL}^{t_{ov}}$, $I_{CL}^{t_{in}}$ are the load currents flowing through C_L at the times t_{ov}, t_{in} in Fig. 15, respectively. Here, $I_{CL}^{t_{ov}}$ can be obtained using (11). Commonly the PMOS transistor works in saturated region because $|V_{GS} - V_{TP}| < V_{DS}$. Thus, the current $I_{CL}^{t_{in}}$ can be approximated as the current I_{D0} of PMOS transistor. Then substituting (23) and (26) into (3), we can obtain the delay time of CMOS inverter.

In some cases, for example, when the load capacitance becomes very small or the input signal transition time is very slow, the t_{50} obtained using (23) and (26) will be smaller than t_{in}. Then the load current is difficult to predict, and the above analysis is not accurate to calculate the rise time. However, as described in [1], the rise time t_r is linearly changed with the input transition time t_{in}. Fig. 16 shows the rise time t_r versus the input transition time t_{in} using the same 32 nm PTM model. It is seen that the rise time t_r almost increases linearly with t_{in}. Fig. 16 indicates that the linear approximation is close to the simulation results. Therefore, the rise time t_r for $t_{in} > t_{50}$ can be approximately expressed as

$$t_r = t_r^0 + \kappa(t_{in} - t_{in}^0) \quad (27)$$

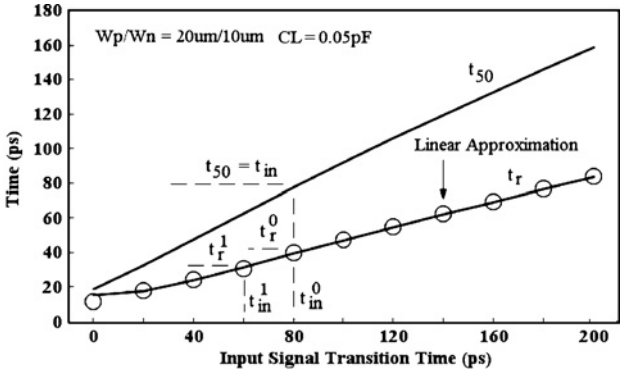

Fig. 16. Rise time t_r versus input signal transition time t_{in}.

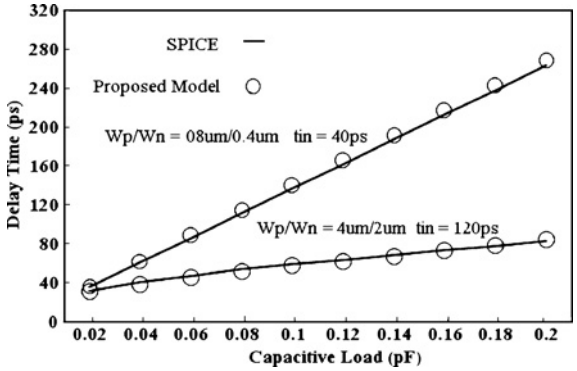

Fig. 17. Comparison of the proposed method and SPICE simulation for various gate drive ability with 32 nm PTM LP model.

where t_r^0 is the rise time that the input transition time t_{in} is equal to t_{50}. Actually, the parameter κ is almost constant and can be obtained with two rise time points as

$$\kappa = \frac{t_r^0 - t_r^1}{t_{\text{in}}^0 - t_{\text{in}}^1} \tag{28}$$

t_r^1 are another rise time point for an input signal t_{in}^1 which is smaller than t_{50}. Substituting (23) and (27) into (3), the delay time is then obtained for $t_{\text{in}} > t_{50}$.

B. Simulation Results

The proposed analytical delay model is first verified with 32 nm PTM high-*k*/metal-gate models for high-performance applications (PTM HP) and for low-power applications (PTM LP) [21], [22].

Fig. 17 shows the comparisons with various NMOS widths from 80 nm to 800 nm with 32 nm PTM LP model. Fig. 18 shows the comparison with respect to the various capacitive load from 0.02 pF to 0.24 pF with 32 nm PTM HP model. From Figs. 17 and 18, it is known that the proposed model is close to SPICE simulation to predict the inverter delay time for various simulation conditions.

The following shows the comparisons of the proposed model with the conventional method in [12] and SPICE simulation. Note that the step input delay times in [12] are obtained from SPICE simulation results. Also pseudoempirical coefficients for delay model are extracted from simulations.

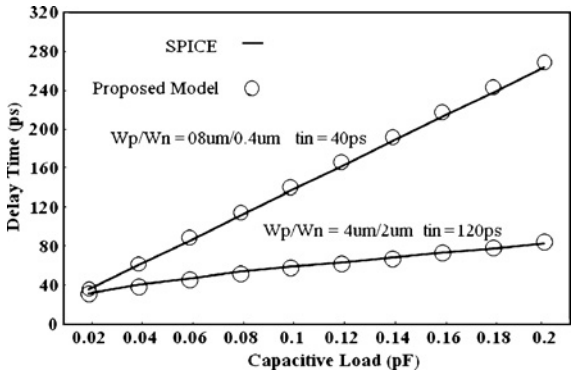

Fig. 18. Comparison of the proposed method and SPICE simulation for various capacitive loads with 32 nm PTM HP model.

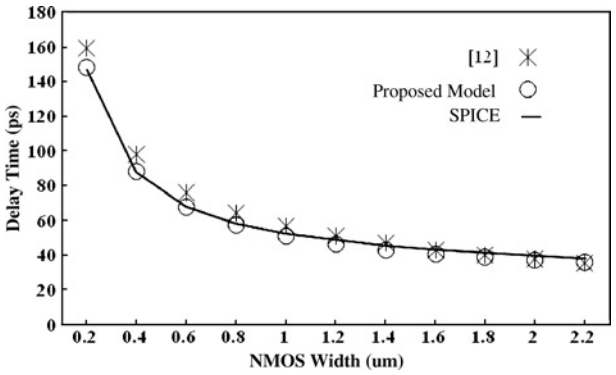

Fig. 19. Comparison of the proposed method, SPICE simulation and [12] for various gate drive ability.

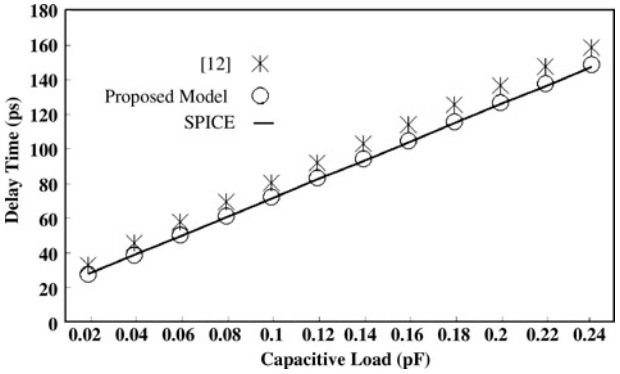

Fig. 20. Comparison of the proposed method, SPICE simulation, and [12] for various capacitive loads.

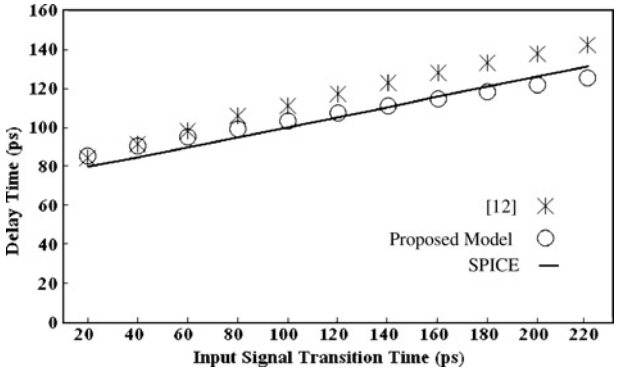

Fig. 21. Comparison of the proposed method with SPICE, [12], and the simple model for various input signal transition times.

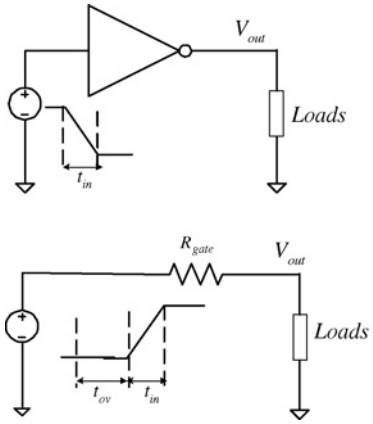

Fig. 22. CMOS inverter with capacitive load and its switch-resistor model.

Fig. 19 shows the comparison with various NMOS widths from 0.2 μm to 2.2 μm. The capacitive load is 0.02 pF and the input transition time is 100 ps. From Fig. 19, it can be seen that the proposed model is close to the SPICE simulation. The average error of the proposed model to predict the delay time is 3.24% while the average error of the delay model in [12] is 6.52%.

Fig. 20 shows the comparison with respect to the various capacitive loads from 0.02 pF to 0.24 pF. The input signal transition time is 50 ps and the size of inverter is that W_p/W_n = 4 μm/2 μm with $L_n = L_p = 40$ nm. The error of the proposed model is within 1.71%. If the conventional method in [12] is used, the error is from 6.71% to 19.57%.

Fig. 21 shows the comparison with various input signal transition times from 20 ps to 220 ps. In Fig. 21, the sizes of inverter transistors are W_p/W_n = 4 μm/2 μm and the capacitive load C_L is 0.05 pF. From Fig. 21, it can be inferred that the proposed method is close to the SPICE simulation with 3.66% average error. The method using the overshooting model in [12] has a 9.66% average error with the increase of the input signal transition time.

From Figs. 19–21, it can be seen that the delay time can be reduced greatly by using large inverter sizes. The delay time increases with respect to capacitive load and input transition time. Since the proposed overshooting effect model is close to SPICE simulation results very well, the proposed analytical model can accurately predict the delay time of CMOS inverter in nanometer technologies.

V. Switch-Resistor Model

In this section, the application of the proposed overshooting time model is discussed to improve the accuracy of the switch-resistor model.

Fig. 22 shows a CMOS inverter driving capacitive loads. The inverter can be modeled as a linear resistor with ramp input voltage for CMOS VLSI circuit analysis, which is called as switch-resistor model. With the scaling of CMOS technology into the nanometer regime, the overshooting time increases and becomes one of the most important parts of CMOS gate output waveform. In [19], the authors proposed a generalized CMOS gate delay model where a shift time t_0 is added to ramp input signal to improve the switching-resistor model. Similar work was also done in [20]. However, the shift time t_0 is not given.

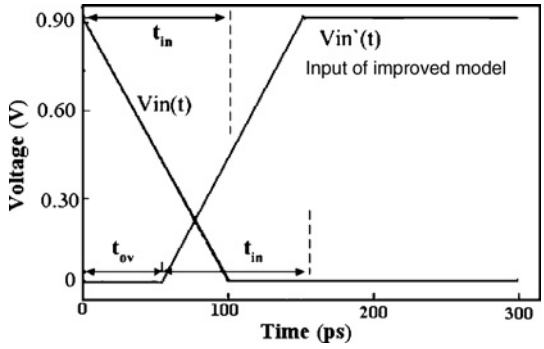

Fig. 23. Improved switch-resistor model.

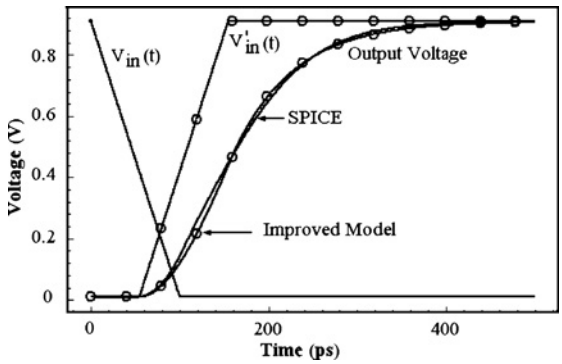

Fig. 24. SPICE simulation and the predictions of the improved switch-resistor model.

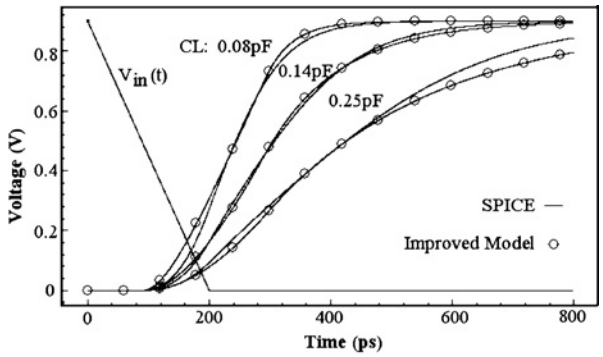

Fig. 25. Simulation results of the improved switch-resistor model to predict the output waveform of an inverter with various capacitive loads.

In this paper, the accuracy of the switch-resistor model is improved while the overshooting effect is considered as shown in Fig. 23. For a ramp input signal $V_{\rm in}(t)$ with $t_{\rm in}$ applied to CMOS inverter, the input signal in the improved model is changed as $V'_{\rm in}(t)$ composed of a shift time $t_{\rm ov}$ and the ramp input with the same $t_{\rm in}$. For the improved model, firstly $t_{\rm ov}$ is obtained using the proposed model to calculate the overshooting time.

Fig. 24 shows the comparison of SPICE simulation and the improved switch-resistor model to predict the output waveform of an inverter with capacitive loads. Note that the linear

resistor in the switch-resistor model is derived by using the SPICE simulation results. From Fig. 24, it can be seen that the improved switch-resistor model can accurately predict the inverter output waveform. Here, the same 32 nm PTM model is utilized in the simulation results.

Fig. 25 shows the simulation results of the inverter when capacitive loads are 0.08 pF, 0.14 pF and 0.25 pF, respectively. From Fig. 25, it can be seen that the switch-resistor model can capture the output waveform of the CMOS inverter with various capacitive loads.

Therefore, the switch-resistor model with the proposed overshooting effect model can be used to predict the output waveform of CMOS inverters. Moreover, the accuracy of switch-models can be enhanced with the assistance use of the transistor-level parameters.

VI. Conclusion

The overshooting effect becomes much larger and cannot be neglected for VLSI analysis with the scaling of CMOS technology into nanometer. In this paper, an effective analytical model has been proposed to estimate the overshooting time for the CMOS inverter delay analysis in nanometer technologies. The accuracy of the proposed model has been proved to greatly agree with SPICE simulation results. Moreover, based on the proposed overshooting time model, an analytical gate delay model has been presented, which is verified to be agreement with SPICE results very well. Furthermore, the accuracy of the switch-resistor model has been improved to predict the inverter output waveform.

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