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An Approach for Reducing Leakage Current Variation due to Manufacturing Variability*****

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SUMMARY Leakage current is an important qualitative metric of LSI (Large Scale Integrated circuit). In this paper, we focus on reduction of leakage current variation under the process variation. Firstly, we derive a set of quadratic equations to evaluate delay and leakage current under the process variation. Using these equations, we discuss the cases of varying leakage current without degrading delay distribution and propose a procedure to reduce the leakage current variations. From the experiments, we show the proposed method effectively reduces the leakage current variation up to 50% at 90 percentile point of the distribution compared with the conventional design approach.

key words: *low power, leakage, gate delay model, variation*

1. Introduction

The power consumption is an important qualitative metric of LSI products. In particular for the battery driven products (e.g. cellular phones, remote control devices, mobile PCs), lower power consumption has to be achieved to be competitive at the market.

The power consumption of CMOS digital circuit consists of i) switching current; dissipated at load capacitance during the active state, ii) short-circuit current; drawn from power line to ground line due to simultaneous ON state of CMOS circuit at the transition state, iii) leakage current; dissipated even in stand-by state. Leakage current has been increasing with advance of technology scaling. In addition, process variation causes vast statistical spread in leakage current at individual chips [1]. It results in lower yield. Reducing the leakage current variation is considered as a very important issue.

The known techniques to reduce power consumption are i) Clock gating to reduce dynamic power dissipations, ii) Multiple-Vdd assignment, iii) Pin reordering, iv) Multiple-Vth assignment. The techniques for leakage current reduction are i) Power gating, ii) Multiple-Vdd assignment, iii) Multiple-Vth assignment, etc. [2]–[4].

The correlation between leakage current and process variation are also studied, e.g. process variation effect [5], leakage current mechanism [6], chip leakage current estimation [7]–[10], components analysis [11], thermal effect [12], correlation analysis between leakage current and delay [1], [13], [14], parametric design approach to reduce the leakage current [15]–[19]. However, the individual effect of each parameter to the total leakage current, or the correlation between delay and leakage current under the process variation were not clarified. Furthermore, leakage current optimization under constant delay constraint was not discussed, so far.

In this paper, firstly, we derive a set of equations to analyze the effect of die-to-die variation on delay and leakage current. Secondly, we quantitatively evaluate the individual effects of each parameter to the total leakage current. Finally, based on the correlation study of delay and leakage current, we propose a procedure to reduce the leakage current variation with keeping the delay variation unchanged.

The rest of paper is organized as follows. In Sect. 2, we show the procedure to derive a set of quadratic equations to analyze the relation between delay and leakage current. In Sect. 3, we validate quadratic models that represent above equations using 45nm technology model. In Sect. 4, we experimentally observe the delay and leakage current relationship. In Sect. 5, based on the studies in Sect. 4, we propose the procedure to reduce leakage current variation while preserving the delay distribution and show the effectiveness of our proposed method in Sect. 6. Section 7 concludes this paper.

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2. Details of Analytical Equations for Delay and Leakage Current

In this section, we detail the procedure to derive analytical representations of delay and leakage current under the process variation.

2.1 Basic Approach

In this paper, we analyze the delay and leakage current of neighboring 2 stages in the series connections of gates to capture the PMOS and NMOS transistor behaviors under rising and falling signal transition states.

We represent delay and leakage current by the following quadratic polynomial using Response Surface Method (RSM).

$$y = \beta_0 + \sum_{i=1}^{n} \beta_i x_i + \sum_{i=1}^{n} \sum_{j \geq i}^{n} \beta_{ij} x_i x_j \tag{1}$$

Here, x_i are variables, β_{ij} are coefficients of quadratic equation, and n is the number of variables. We use threshold voltage V_{th}, Channel length L, and Gate oxide thickness T_{ox} as variables, since these parameters are assumed to contribute the delay and leakage variations. Channel width W and mobility μ can be captured in a similar way by increasing the number of variables.

2.2 Delay Equation

The analytical expression of CMOS inverter delay is approximated using the α-power law model [20].

$$T_d = \frac{C_L V_{dd}}{\mu \cdot \frac{\epsilon_{ox}}{T_{ox}} \cdot \frac{W}{L} (V_{dd} - V_{th})^{\alpha}} \tag{2}$$

Here, C_L is the load capacitance, V_{dd} is a supply voltage, ϵ_{ox} is the dielectric permittivity of gate oxide, α is a constant for an individual process technology (normally takes the value in the range of [1, 2].) Thus, the above relationship can be represented as follows.

$$T_d \propto \frac{1}{(V_{dd} - V_{th})^{\alpha}} L T_{ox} \tag{3}$$

Here, T_d can be expressed by the quadratic equation of V_{th} since α approximately takes the value in the range of [1, 2]. Now we express the delay as follows using Eq. (1) and above relations.

$$T_{d,1} - T_{d,0} = f\Bigg(V_{th,P,1} - V_{th,P,0}, V_{th,N,1} - V_{th,N,0}, \frac{L_{P,1}}{L_{P,0}}, \frac{L_{N,1}}{L_{N,0}}, \frac{T_{ox,P,1}}{T_{ox,P,0}}, \frac{T_{ox,N,1}}{T_{ox,N,0}} \Bigg) \tag{4}$$

Here, $T_{d,1} - T_{d,0}$ corresponds to the response y in Eq. (1). The variables of function f correspond to variables x_1–x_6 by assigning n as 6 in Eq. (1). Subscripts P, N, 0, and 1 indicate PMOS transistor, NMOS transistor, nominal state, and varied state, respectively.

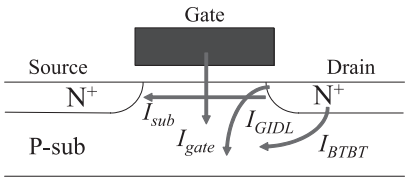


Fig. 1 Leakage current components.

2.3 Leakage Current Equation

The total leakage current can be approximately expressed by the sum of individual leakage current components [4].

$$I_{total} = I_{BTBT} + I_{sub} + I_{gate} + I_{GIDL} \tag{5}$$

Here, I_{BTBT} is the reverse-biased source-drain PN junction current, I_{sub} is the sub-threshold leakage current, I_{gate} is the gate current due to tunneling current and hot carrier, and I_{GIDL} is a drain current due to high voltage field effect. Each factor is schematically shown in Fig. 1. According to BSIM4 [21], I_{sub} can be expressed as follows.

$$I_{sub} = \mu \cdot \frac{\epsilon_{ox}}{T_{ox}} \cdot \frac{W}{L} \cdot V_T^2 \cdot e^{\frac{V_{gs} - V_{th}}{m V_T}} \cdot \left(1 - e^{\frac{-V_{th}}{V_T}}\right) \tag{6}$$

Here, $V_T = kT/q$(V) where k is the Boltzmann constant 1.38054×10^{-23} (eV/k), T is the absolute temperature, and q is a charge of electron 1.6×10^{-19} (Q). m is a coefficient and V_{gs} is a voltage difference between gate-source nodes of transistor. From Eq. (6), logarithm of I_{sub} has the following relation.

$$\ln(I_{sub}) = \frac{1}{m V_T}(V_{dd} - V_{th}) - \ln(T_{ox}) - \ln(L) + \cdots \tag{7}$$

Here, V_{dd} is a supply voltage to a source node of transistor. We assume the dominance of I_{sub} in the total leakage current [11]. Thus the leakage current can be expressed as follows using Eq. (1) and above relations.

$$\ln\left(\frac{I_{leak,1}}{I_{leak,0}}\right) = g\Bigg(V_{th,P,1} - V_{th,P,0}, V_{th,N,1} - V_{th,N,0}, \frac{L_{P,1}}{L_{P,0}}, \frac{L_{N,1}}{L_{N,0}}, \frac{T_{ox,P,1}}{T_{ox,P,0}}, \frac{T_{ox,N,1}}{T_{ox,N,0}} \Bigg) \tag{8}$$

Here, $\ln(I_{leak,1}/I_{leak,0})$ corresponds to the response y in Eq. (1). The variables in function g correspond to variables x_1–x_6 by assigning n as 6 in Eq. (1).

Since Eqs. (4) and (8) consist of same variables, we can analyze the relation between delay and leakage current depending on device parameters using these quadratic equations.

3. Extract Coefficients of the Equations

3.1 Experimental Setup

Experimental parameter conditions to extract the coeffi-

Table 1 Details of experimental conditions.

Tr.	Model	BSIM4 [21]
	Process	PTM 45(nm), Typical [23]
	PMOS	L=45 (nm), W=450 (nm)
	NMOS	L=45 (nm), W=225 (nm)
Variation (3σ/μ) [22]	V_{th}	42%
	L	12%
	T_{ox}	4%
V_{dd}	1.0(V)	
temp.	25(℃)	

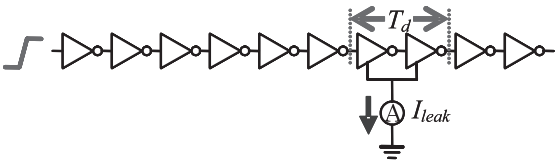


Fig. 2 An experimental circuit setup.

Table 2 Extracted coefficients β_{ij} of delay equation for CMOS inverter.

i \ j	0	1	2	3	4	5	6
0	2.38E-11	3.07E-11	-3.08E-11	-7.54E-11	-2.51E-11	-1.81E-11	-1.09E-11
1		2.38E-11	2.30E-11	3.77E-11	4.00E-11	1.05E-11	1.49E-11
2			-8.70E-11	-8.61E-12	3.00E-11	3.29E-11	1.36E-11
3				-2.86E-11	-2.67E-11	8.86E-12	2.32E-11
4					8.51E-12	3.93E-12	3.35E-12
5						-4.72E-11	3.18E-12
6							-4.02E-11

cients of Eqs. (4) and (8) are listed in Table 1. The variation ranges of V_{th}, L, and T_{ox} are cited from ITRS [22]. SPICE model parameters are obtained from PTM [23]. We have chosen 5-level experiment $\{-3\sigma, -\sigma, 0, \sigma, 3\sigma\}$ for six parameters, i.e. V_{th}, L, and T_{ox} of PMOS and NMOS, which produces $5^6 = 15625$ times of SPICE simulation in result. Experimental circuit is a multiple stage of CMOS inverters as shown in Fig. 2. We here assume that the two inverters of our interest are perfectly correlated for each variation parameter, since they are expected to be placed adjacently. Two stages of delay (T_d) and leakage current (I_{leak}) are obtained from the simulations and each coefficient is extracted through the linear least-squares fitting.

3.2 Extraction Results

The extracted coefficients are shown in Tables 2 through 5. In the tables, indices of the coefficients correspond to the variables in Eqs. (4) and (8). β_{ii} and β_{ij} correspond to the β_i and β_{ij} in Eq. (1), respectively. Tables 2 and 3 show the coefficients in the cases of all the 6 parameters (V_{th}, L, and T_{ox} of NMOS and PMOS transistors) are varied. Tables 4 and 5 show the cases of V_{th}, L, and T_{ox} are individually varied. For example, the coefficients of V_{th} in the tables are obtained from 25 times of simulation with varying V_{th} parameters of PMOS and NMOS transistors while fixing L and T_{ox} parameters as mean values. They will be used to analyze the individual parameter effect on correlation of PMOS and NMOS transistors in Sect. 5.

Table 3 Extracted coefficients β_{ij} of leakage current equation for CMOS inverter.

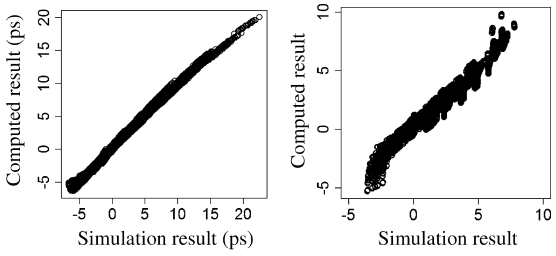
i \ j	0	1	2	3	4	5	6
0	6.17E-01	1.02E+01	-8.80E+00	-1.57E+01	-1.10E+01	-1.03E+00	-2.53E+00
1		1.79E+01	3.06E+01	-3.77E+01	3.57E+01	-8.35E+00	1.31E+01
2			1.58E+01	-4.35E+01	3.37E+01	-3.37E+00	-5.51E-01
3				7.98E+01	-5.30E+01	-7.18E+00	-1.58E+01
4					5.55E+01	-3.79E+00	-1.37E+01
5						4.44E-01	-1.64E+00
6							3.85E+00

Table 4 Extracted coefficients β_{ij} of delay equation for CMOS inverter when each parameter was individually varied.

V_{th}	β_0	β_1	β_2	β_{11}	β_{22}	β_{12}
	-6.42E-15	-1.86E-11	1.63E-11	3.01E-11	2.35E-11	-2.97E-11
L	β_0	β_3	β_4	β_{33}	β_{44}	β_{34}
	-5.27E-11	2.20E-11	4.04E-11	-9.73E-12	-2.53E-11	2.54E-11
T_{ox}	β_0	β_5	β_6	β_{55}	β_{66}	β_{56}
	-2.98E-12	-3.29E-12	-1.68E-12	2.87E-12	2.43E-12	2.65E-12

Table 5 Extracted coefficients β_{ij} of leakage current equation for CMOS inverter when each parameter was individually varied.

V_{th}	β_0	β_1	β_2	β_{11}	β_{22}	β_{12}
	2.26E-01	1.14E+01	-9.43E+00	3.21E+01	2.66E+01	4.37E+01
L	β_0	β_3	β_4	β_{33}	β_{44}	β_{34}
	1.42E-01	-1.88E+01	-1.34E+01	1.14E+02	8.34E+01	-9.11E+01
T_{ox}	β_0	β_5	β_6	β_{55}	β_{66}	β_{56}
	-6.36E-06	-1.60E+00	-2.29E+00	9.17E-01	6.33E+00	-3.64E+00



(a) $T_{d,1}$-$T_{d,0}$ (b) $\ln(I_{leak,}/I_{leak,0})$

Fig. 3 Accuracy evaluation results of analysis equations. (a) Comparison between simulation and computed results of delay equation. (b) Comparison between simulation and computed results of leakage current equation.

3.3 Accuracy of the Equations

Figure 3 shows the comparison results of SPICE simulation and computed results of the equations for delay and leakage current. Adjusted R-squared values of delay and leakage current are 0.995 and 0.968, respectively. More than the value of 0.95 are shown in the cases of parameters which are varied individually, or NAND and NOR cases referred in the latter section. Our models are accurate to analyze the trend of delay and leakage current due to process variation.

4. Characteristics of Leakage Current under Process Variation

In this section, we experimentally observe the process variation effect to the leakage current variation.

4.1 Process Variation Effect to Leakage Current

Figure 4 shows the effect of process variation to the leakage current from SPICE simulations. In the figure, horizontal and vertical axes are variations based on Table 1 and resulting variation ratio to nominal case, respectively. In the experiments in this section, we assume the perfect correlation between PMOS and NMOS transistors. The figure shows that the effects of T_{ox} variation are clearly small.

4.2 The Correlation of Delay and Leakage Current due to Process Variation

Figure 5 depicts the scatter plots between delay and leakage current according to the V_{th}, L, and T_{ox} variations listed in Table 1. In the figure, horizontal and vertical axes are delay and logarithm of leakage current, respectively. Each of measurement point is obtained from 10,000 analysis of SPICE Monte Carlo simulation. The figure clearly shows that the leakage current varies for a constant delay, which is shown in literature [7] from the actual measurement result. In other words, leakage current variations are possibly optimized under constant delay constraint. We focus on this relation, investigate leakage current and delay distribution, research the parameter conditions which vary leakage current while maintaining the delay distribution, and reduce its leakage current variations.

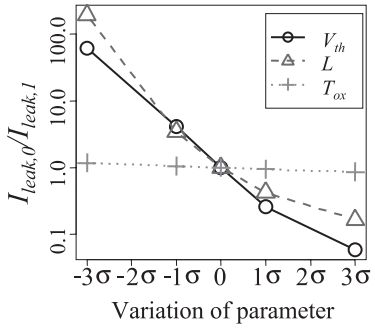


Fig. 4 Individual effects of process parameter variation to leakage current variation.

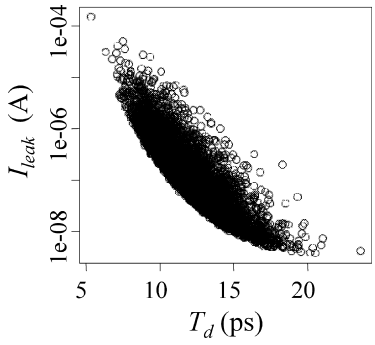


Fig. 5 Scatter plot between delay and logarithm of leakage current under the process variation.

5. Approach to Reduce Leakage Current Variation

In this section, we detail the procedure to minimize leakage current while preserving delay and show that the proposed procedure reduces leakage current variation successfully.

5.1 Analyze the Relation between Delay and Leakage Current

The projection of the delay or leakage current equations on two dimensional parameter spaces depicts an oval distribution from their quadratic approximation. Here, we use V_{th} parameters of NMOS and PMOS transistors ($V_{th,P}$ and $V_{th,N}$, respectively) as an example. The coefficients of the equations are referred from Tables 4 and 5.

Figure 6(a) depicts delay and leakage current distribution. In the figure, horizontal and vertical axes are PMOS and NMOS V_{th} parameters differences from nominal value, respectively. Figure 6(b) depicts L parameter case instead of V_{th} parameter. Solid and bold lines are the contour of delay and leakage current, respectively. The lines labeled as 0 represent the combination of parameters to keep delay or leakage current values of the current design.

Moving the nominal values of parameters along the delay contour line labeled 0 results in the change of leakage current variation while keeping the delay. Conversely, minimal leakage current condition of the parameters can be obtained by scanning the delay contour line.

The figures show the minimum leakage current condition close to the initial parameter combination which is not always expected. In the cases that initial parameter condition differs from minimal leakage current condition, the procedure above can be used to minimize leakage current without affecting delay.

Note here that reduced leakage current variation can be expected by the procedure above. The concept of this idea is schematically shown in Fig. 7. The figure shows delay and leakage current contour lines in the similar manner of Fig. 6. In the figure, initial and revised parameter combinations are

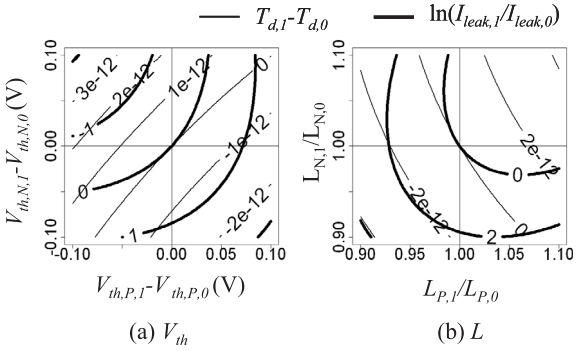


Fig. 6 Contour of delay and leakage current of CMOS inverter with shifting nominal values of process parameters. (a) Shifting V_{th} parameter of NMOS and PMOS transistors. (b) Shifting L parameter of NMOS and PMOS transistors.

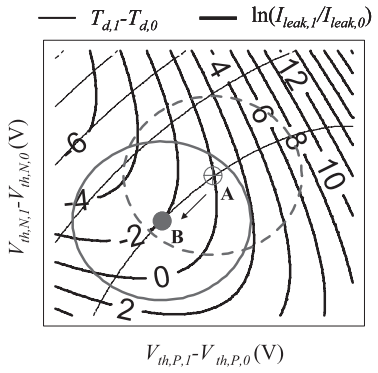


Fig. 7 The concept of reducing leakage current variation by reducing nominal leakage current value.

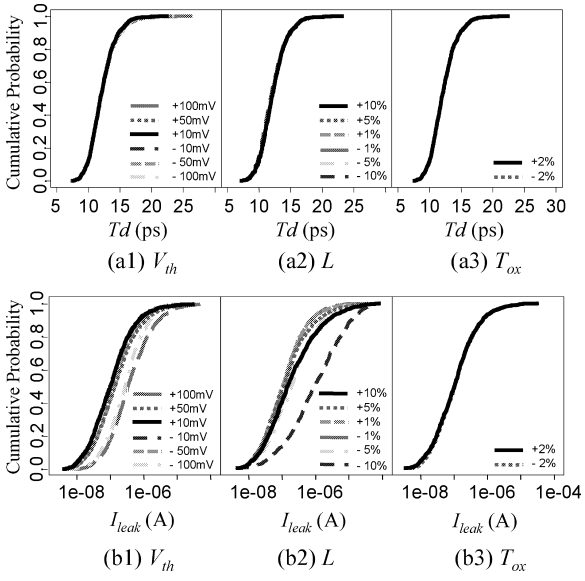


Fig. 8 Cumulative distributions of delay and leakage current of CMOS inverter with shifting nominal values of process parameters. (a1) delay with shifting V_{th}. (a2) delay with shifting L. (a3) delay with shifting T_{ox}. (b1) leakage current with shifting V_{th}. (b2) leakage current with shifting L. (b3) leakage current with shifting T_{ox}.

marked as A and B, respectively. The solid and dashed circle lines having same radius around the positions showing the equivalent probability contour from their Gaussian approximation, and their distributions vary equally. The distribution of A clearly varies in the higher leakage current area. Thus moving nominal parameter condition A to B results in reduced leakage current variation.

5.2 Reduce Leakage Current Variation while Maintaining Delay Distribution

In the former section, we discussed that reduced leakage current variation is expected by minimizing the mean value of leakage current. In this section, we will confirm the scenario with intentionally varying the NMOS and PMOS transistor parameters.

Figure 8 shows a cumulative distribution of delay and leakage current from the result of SPICE Monte-Carlo analysis. In the analysis, V_{th}, L, and T_{ox} parameters are individually varied according to the procedure detailed in Sect. 5.1. In the experiments, we altered the parameters listed in Table 1 to the direction of increasing the resulting variation to observe the variation effect clearly. The amount of alternations are $\{\pm 10\,\mathrm{mV}, \pm 50\,\mathrm{mV}, \pm 100\,\mathrm{mV}\}$, $\{\pm 1\%, \pm 5\%, \pm 10\%\}$, and $\{\pm 2\%\}$ for V_{th}, L, and T_{ox} parameters of NMOS transistor, respectively. The ones of PMOS transistor are deliberately chosen to maintain delay constant for each set of NMOS parameters, where the PMOS and NMOS parameters are often in the opposite direction in terms of delay and leakage performance. The figure shows that leakage current distributions (lower side) are varied while the delay distributions (upper side) are preserved, this characteristic matches our expectation. It has been shown that minimizing leakage current results in reducing leakage current variation. The figure also shows that leakage current is less sensitive to T_{ox} parameter variation which agrees with the result in Sect. 4.1.

5.3 Analytical Approach

In the above, we have found the parameter combination to reduce leakage current variation by the observations of drawn graphs. To find the parameter combination analytically, Lagrange multipliers method can be used. Here, we show the 2 variables case as an example. Now the leakage current and delay equations are expressed as follows.

$$\ln\left(\frac{I_{leak,1}}{I_{leak,0}}\right) = a_1x_1 + a_2x_2 + a_{11}x_1^2 + a_{22}x_2^2 + a_{12}x_1x_2 \tag{9}$$

$$T_{d,1} - T_{d,0} = b_1x_1 + b_2x_2 + b_{11}x_1^2 + b_{22}x_2^2 + b_{12}x_1x_2 \tag{10}$$

The problem to obtain the extreme values of leakage current while keeping the value of $T_{d,1} - T_{d,0}$ as 0 turns into solving the following simultaneous quadratic equations. The smaller solution is an expected answer.

$$\begin{aligned} &a_1b_2 - a_2b_1 \\ &\quad + (a_1b_{12} + 2a_{11}b_2 - a_{12}b_1 - 2a_2b_{11})\cdot x_1 \\ &\quad + (a_{12}b_2 + 2a_1b_{22} - a_2b_{12} - 2a_{22}b_1)\cdot x_2 \\ &\quad + (2a_{11}b_{12} - 2a_{12}b_{11})\cdot x_1^2 \\ &\quad + (2a_{12}b_{22} - 2a_{22}b_{12})\cdot x_2^2 \\ &\quad + (4a_{11}b_{22} - 4a_{22}b_{11})\cdot x_1\cdot x_2 = 0 \end{aligned} \tag{11}$$

$$b_1x_1 + b_2x_2 + b_{11}x_1^2 + b_{22}x_2^2 + b_{12}x_1x_2 = 0 \tag{12}$$

The analytical results of V_{th} and L cases are ($V_{th,P,1} - V_{th,P,0}$, $V_{th,N,1} - V_{th,N,0}$)=(0.003, 0.003) and ($L_{,P,0}/L_{,P,1}$, $L_{,N,1}/L_{,N,0}$) =(0.995, 1.01), respectively. These results are very close to the initial conditions, which tendency is same as the results observed in Sect. 5.1.

6. Effectiveness of Proposed Procedure

In this section, we present application examples for 2-input NAND and 2-input NOR gates. Experimental conditions and parameters in Fig. 2 and Table 1 are unchanged except that the CMOS inverters are replaced by the target logic gates. One of the two input pins of the replaced gates is tied to logical High or Low to enable signal propagation.

Figure 9 depicts the contour maps of delay and leakage current as functions of threshold voltages of NMOS and PMOS transistors. The lines are obtained by the proposed procedure. The minimum leakage-current point marked with black circles are different from the current condition, showing that there exists room for optimization by further investigating designs as discussed later in this section.

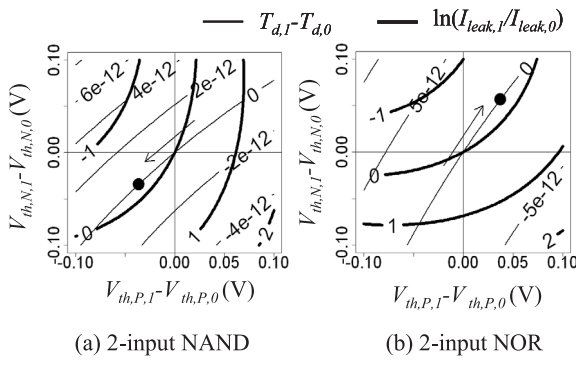


Fig. 9 Contour of delay and leakage current with shifting V_{th} parameter of NMOS and PMOS transistor. (a) Result of 2-input NAND gate. (b) Result of 2-input NOR gate.

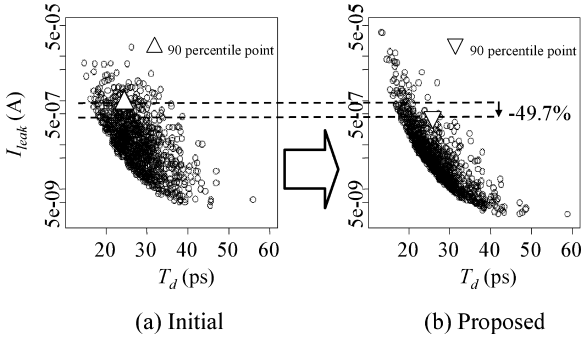


Fig. 10 Scatter plot between delay and leakage current of 2-input NOR gate. (a) Initial parameter condition of each process parameter. (b) Revised parameter condition by our proposed method.

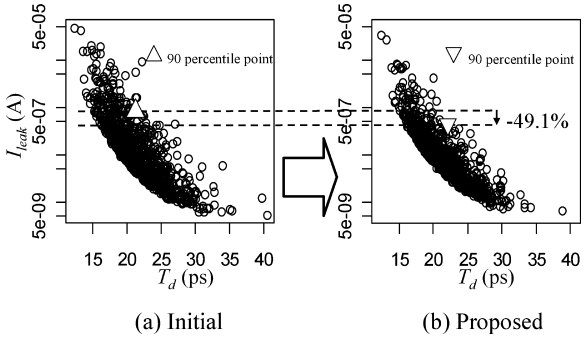


Fig. 11 Scatter plot between delay and leakage current of 2-input NAND gate. (a) Initial parameter condition of each process parameter. (b) Revised parameter condition by our proposed method.

Figures 10 and 11 show the SPICE-simulated change of delay and leakage current for NOR and NAND gates, respectively. In both figures, (a) and (b) correspond to initial and optimized conditions, respectively. In the experiments, all the 6 parameters (V_{th}, L, and T_{ox} of PMOS and NMOS transistors) are adjusted to reduce leakage current variation while maintaining the delay distribution. The figures show that the reductions of leakage current variation are 49.7% and 49.1% at the 90 percentile point of the distribution in the NOR and NAND cases, respectively. Our proposed procedure can reduce the leakage current variation effectively by applying to individual cell types. The procedure can be applied even in the middle of chip design phase, since it maintains the delay distribution.

Note here that the minimum leakage current conditions for different logic gates can possibly become contradicting as we have observed in Fig. 9. However, the proposed procedure is still useful to reduce leakage currents. 1) In standard cell design phase, gate length L and width W are design parameters, and hence each cell or even each instance can be tweaked by adjusting L and W with the proposed procedure. 2) Instead of assigning optimal V_{th} and T_{ox} for individual cells, which may be doable such as by using multiple body-bias voltages but unrealistic, we can assign V_{th} and T_{ox} to achieve overall optimization. That is, cell utilization can be analyzed for a particular design in order to strategically apply the proposed optimization flow for gaining the maximum leakage reduction while satisfying the speed specification. 3) Moreover, design-dependent optimization flow based on our procedure can be constructed so that the flow simultaneously considers the analytical representation of a critical path delay as in Eq. (1) and leakage-dominant cells within a chip.

7. Conclusion

In this paper, we presented a methodology for reducing the leakage current variation under constant delay constraint. Firstly, we derived the quadratic equations to analyze delay and leakage current variations and verified them using 45 nm technology model. Secondly, we proposed the procedure to reduce leakage current variation while maintaining delay distribution and experimentally showed that our proposed method effectively reduces leakage current variation up to 49.7%. We also discussed the application of our proposed method in design and process manufacturing phase.

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