Interconnect Modeling: A Physical Design Perspective

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(Invited Paper)

***Abstract*—Variability, reliability, and design size are becoming major difficulties in system-on-a-chip (SoC) designs as the scaling of semiconductor technology advances. Techniques for interconnect modeling and analysis in designing advanced SoCs are discussed from the design-automation point of view. Importance of interconnect modeling in modern chip-design flows is first summarized. State-of-the-art physical-design techniques for parasitic extraction, signal-integrity analysis, and timing analysis (which are commonly executed throughout the final verification of physical design) are then reviewed. The extraction and analysis require the most accurate process information and modeling. Requests with respect to the manufacturing–design interface are discussed, and the authors' perspective concerning future SoC physical designs is addressed with emphasis on interactions between manufacturing and design technologies.**

***Index Terms*—Interconnect, parasitic extraction, process variation, signal integrity, timing analysis.**

I. Introduction

INTERCONNECTS are an important constituent of an LSI, and interconnect modeling is becoming increasingly more important. The continuous progress of semiconductor technology is leading system-on-a-chip (SoC) to the era of 45-nm technology and beyond. Given the huge number of devices and interconnects integrated in a modern LSI [1], the requirement of shorter design time is a crucial challenge. The increasing variability of the manufacturing-process parameters makes the challenge even more difficult. In regard to modern LSI designs, it is fundamentally important to develop a design environment that realizes *reasonable* modeling and analysis in terms of both computation complexity and accuracy. It is also important to develop an optimal design methodology with which products are guaranteed to operate in all fabrication plants (fabs) while sharing the same design technology.

Issues concerning manufacturing variability and reliability are causing increasing difficulties in advanced SoC designs. The integration of low-k dielectric and low-resistivity metals is a key factor in reducing delay and power consumption. High-accuracy critical-dimension control [2] restrains variability, and increased reliability eradicates temporal defects such as electromigration (EM) [3], stress-migration (SM) [4], and time-dependent dielectric breakdown [5]. Current lithography is supported by resolution-enhancement techniques such as optical proximity correction, subresolution assist features, off-axis illumination, and phase-shifting mask [1], [6]. Interconnect variability arises in the lithography process and other processes such as etching and chemical–mechanical polishing (CMP). In addition, the technology scaling inevitably induces an increase in effective resistivity by grain-boundary and surface scattering. Moreover, reducing barrier-metal thickness accurately, which further increases resistivity and resistivity variation, is difficult. Manufacturing techniques to solve these issues are required to have a tight link with design technologies as they often place restrictions on design rules.

Design technologies have been developed to solve some of the manufacturing issues aforementioned. Methodologies like design for manufacturability (DFM) or design for yield (DFY) have been intensively studied [7]–[10]. Examples are insertion of dummy metal fills for helping planarization during CMP [11], redundant vias (e.g., double vias) [7] for relieving via defects, and wire spreading/widening [8] for preventing metal shorts/opens. To reduce design-dependent variations, a methodology that incorporates a CMP simulator and lithography simulator in a design flow has been also studied [12]. With the advancement of semiconductor technology, impact of interconnect resistance and capacitance on circuit operations is becoming significant. Accordingly, it is becoming commonplace to consider interconnect variability in a design flow, particularly in parasitic extraction [13], [14] and signal-integrity [15] and timing analyses [16], [17]. In a modern chip-design flow, timing analysis is the most critical verification step for ensuring correct circuit operations. Corner-based static timing analysis (STA) [18] has been widely used as the standard timing analysis. Recently, STA considering on-chip variation (OCV), spatial correlation, and logic-depth-dependent canceling effect has been widely used [18]. For a more accurate statistical

Manuscript received January 16, 2009; revised June 16, 2009. First published July 28, 2009; current version published August 21, 2009. This work was supported by the IEEE. The review of this paper was arranged by Editor M. J. Deen.

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Digital Object Identifier 10.1109/TED.2009.2026208

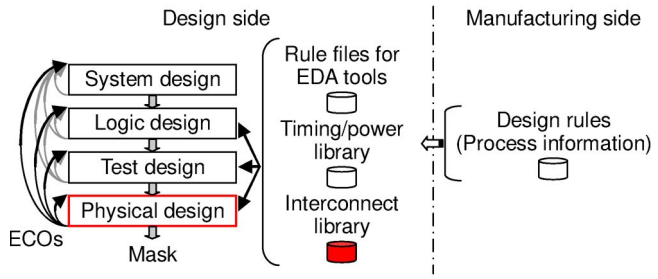

Fig. 1. Overview of SoC design flow.

treatment, statistical STA (SSTA) [16], [19], [20] is becoming a mainstream tool. In such a design environment, process information (including variability [21]) is critical. Accuracy of the process information determines the quality of variation-, yield-, and reliability-aware designs and, thus, strongly influences the profit of a SoC product.

In this paper, we discuss interconnect modeling and analysis, with emphasis on interactions between manufacturing and design technologies. The rest of this paper is organized as follows. Section II reviews the importance of interconnect modeling in a design flow. Sections III–V describe design technologies related to interconnect effects, including interconnect parasitic extraction, signal-integrity analysis, and timing analysis, respectively. The prospected manufacturing–design interface from a design perspective is discussed in Section VI followed by the conclusion in Section VII.

II. Importance of Interconnect Modeling in Design Flow

Fig. 1 shows a typical design flow for a SoC. The flow is generally divided into two phases: front-end design of the system, logic, and testing and back-end design for physical implementation of a SoC. The focus of this paper is on the back-end design, hereinafter referred to as the physical design. A modern SoC is composed of hard macroblocks and random logics. The hard macroblocks are input and output (I/O) buffer cells, memories, analog circuits, etc., which are prepared and used as layout entities. The random logics are further divided into two: soft macroblocks such as a digital signal processor or a central processing unit (CPU) (which are synthesized specifically for each SoC design) and glue logics (which connect the hard and soft macroblocks). The specific topic covered in this paper is about the design of random logics.

Design rules shown in Fig. 1 include interconnect layout rules such as those for spacing, wire width, and metal density. Process information such as SPICE model parameters and interconnect cross-sectional dimensions is also provided. Based on that information, the libraries used by EDA tools are generated. The timing/power library contains delay and power information of standard logic cells and hard macroblocks. The library is constructed through comprehensive SPICE simulations with various conditions based on sets of SPICE model parameters. The interconnect library contains templates of interconnect parasitic $R(L)C$ values for various interconnect structures. The templates are obtained by executing a field solver with many combinations of cross-sectional dimensions and material properties. These libraries are referred to intensively throughout

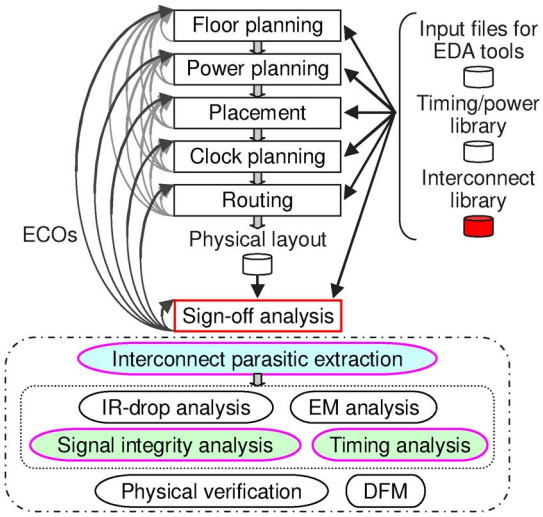

Fig. 2. Procedures involved in physical design and the sign-off analysis.

the physical-design steps. Consequently, information provided by the manufacturing side is crucially important.

Fig. 2 shows a representative procedure involved in physical design. Considering interconnect length and congestion, floor planning defines rough locations for hard macroblocks and random logic areas. In power planning, power and ground distributions such as power rings and grids are generated so that the voltage drop (IR drop) due to interconnect parasitics is minimized. Placement of standard logic cells considers length and congestion of interconnects. Clock planning and routing realize all wire connections.

Sign-off analysis is the final verification step that determines whether the design can be passed to the fabrication process or not. Interconnect parasitics are first extracted by pattern matching that consults the interconnect library or, occasionally, with the aid of field solvers. The variation of parasitic values is accounted for during the extraction procedure. Based on the extracted parasitics, IR-drop analysis, EM analysis, signal-integrity analysis, and timing analysis are conducted. Among these, the signal-integrity and timing analyses are highly sensitive to interconnect parasitic values; thus; those analyses are also conducted during the logic and test-design phases, as shown in Fig. 1, by consulting the respective libraries. Engineering change orders (ECOs) for partial modifications are iterated in most of the phases shown in Figs. 1 and 2. In this paper, an ECO is a small design change that alters a small portion of the circuits, placement, routing, etc., while the majority of the design portions are kept unchanged. The EDA tools must handle ECOs very efficiently, since ECOs are issued many times before a chip design is completed. Simple yet accurate interconnect modeling is therefore important.

It is also important for designers to have accurate interconnect information, since the libraries fully rely on the information presented. Uncertain information may cause unreliable circuit operation, which becomes known only after the fabrication of the SoC. Of course, a successful design also relies on accurate analysis tools and effective design methodologies. As well as the circuit design, the modeling and analysis of interconnects also determine circuit operation, reliability, and chip cost. In the next three sections, recent techniques for

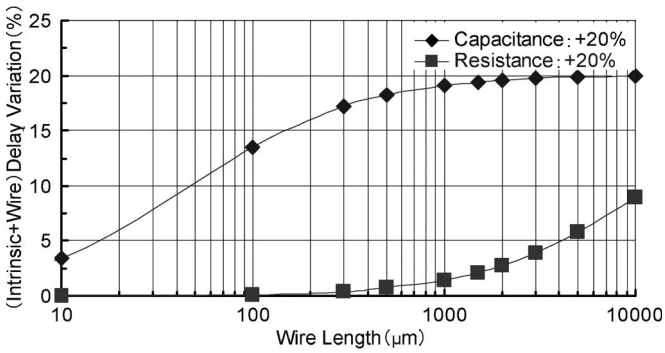

Fig. 3. Interconnect-delay variation versus wire length for 20% change in R and C.

modeling and analysis used in physical design and verification are reviewed.

III. Interconnect Parasitics

In addition to the influence of interconnects on circuit performance becoming large, it is becoming difficult to manufacture interconnects as designed shapes by nanoscale wafer processes. Since interconnect resistance and capacitance are both affected by wire width, spacing, and thickness of metals and dielectric films, they have strong influence on signal-propagation delay and crosstalk noise. Moreover, as the 3-D structure of the wires becomes complicated, it becomes difficult to extract the parasitics of the interconnects, leading to an increase in the uncertainty of delay estimation. In addition, increase in operating frequencies necessitates the handling of high-speed signals in an LSI. On-chip inductance, which could be ignored because of the relationship between wire length, wavelength, and signal transition time, is beginning to affect the propagation characteristic of the signals.

This section discusses the extraction of the interconnect parasitics that should be considered in designing a SoC with current and future wafer processes.

A. Interconnect Library

With the progress in wafer-process technology, it has become impossible to ignore OCVs of interconnect delay. The variation also affects the analysis of signal-integrity issues. Smaller on-chip wire pitch increases delay and crosstalk noise because it increases parasitic capacitance [13]. Fig. 3 shows an example of the delay variation in a commercial 90-nm SoC process against wire length when interconnect resistance and capacitance increase by 20%. As shown in the figure, precise estimation of capacitance is important when evaluating signal-propagation delay.

Most interconnect-parasitic-extraction programs use pattern-matching methods that find a suitable primitive pattern in a precharacterized library, where each primitive is characterized using a field solver. A typical procedure for primitive pattern matching is as follows.

Step 1) Isolate geometries.
Step 2) Allocate region of capacitance extraction for each geometry.

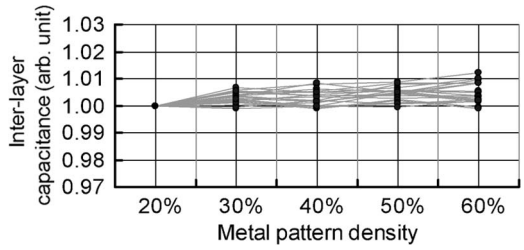

Fig. 4. Variation of plate capacitance (Cv) with respect to pattern density of each single layer (M2–M5).

Step 3) Decompose each region into primitives.
Step 4) Look up primitives in characterized library.
Step 5) Combine primitive information to create an electric equivalent circuit model.
Step 6) Build the network and apply reduction for output.

In this paper, the major sources of errors are steps 3) and 4). In step 3), the boundary condition of each primitive becomes different from the original region. In step 4), errors are introduced by interpolation because the number of primitives is finite. The number of primitives in the library is determined according to a tradeoff between accuracy and library characterizing time. Hence, to determine variation of primitives, making use of regularities in design is helpful.

In interconnect parasitic extraction, it is important to know the precise values of interconnect cross-sectional geometries. Since controlling the shape of fabricated interconnects is becoming increasingly difficult, it is important to monitor actual geometries of the fabricated interconnects in order to understand their statistical distribution. The widely used measurements by scanning electron microscope (SEM) or transmission electron microscope (TEM) are restricted in terms of the availability of samples. Moreover, the measured values unavoidably include random components [22], making it difficult to estimate a nominal value with a small number of samples. Furthermore, the fragileness of recently introduced low-k insulation materials make observations by SEM or TEM even more difficult. It is thus necessary to establish a way to estimate the nominal geometry of each interconnect while excluding the effect of variability [14].

A nondestructive metrology that accurately estimates cross-sectional physical parameters of LSIs was proposed in [13], and it has been successfully applied to copper-interconnect structures fabricated in the 90-nm SoC wafer process. Dimensions of both insulation films and wires are estimated from the measurements of interconnect capacitance and resistance. The proposed method first prepares capacitance lookup tables by using a field solver, for a set of interconnect structures with the actual shapes of wires calibrated using charge-based capacitance-measurement method [23]. It then builds response surface functions (RSFs), in which the capacitance and the resistance values are the responses and the physical parameters are the variables. Finally, using the RSFs, the method searches for a set of physical parameters that most likely matches the measured capacitance and resistance by employing the simulated annealing.

The total number of required test structures depends on the deterministic variation of parameters, such as pattern-density

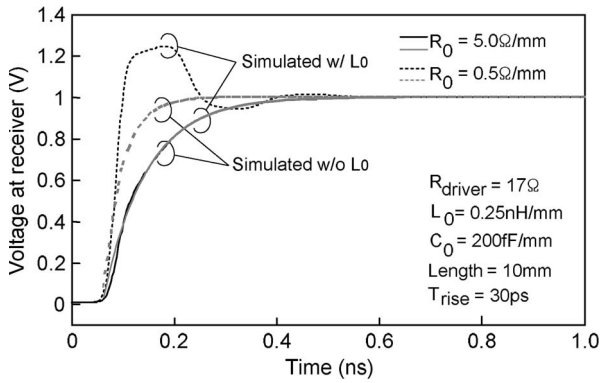

Fig. 5. Signal behaviors on interconnects with different resistivity.

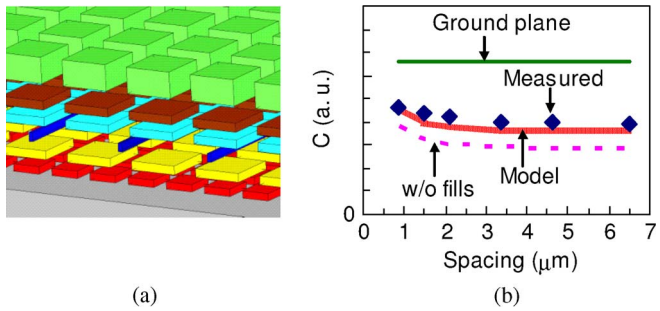

Fig. 6. Comparison of the capacitances simulated by the model and those measured from a test chip. (a) Three-dimensional view of interconnects. (b) Measured and modeled capacitance versus spacing between signal lines.

dependence [24]. In the 90-nm process, only 16 test structures with different wire width and spacing for each layer are sufficient because of the weak dependence of pattern density, as shown in Fig. 4 [13]. This means that the CMP process [25] enables the thickness of copper wires to be practically treated as uniform in the particular process. In future wafer processes, it will be important to evaluate the deterministic variations and then determine the most suitable method to estimate actual values of interconnect cross-sectional parameters.

B. On-Chip Inductance

On-chip interconnect inductance is of concern in regard to implementing high-performance LSIs [26], [27]. That is, on-chip inductance becomes important with faster rise times and lower wire resistance [28]. Typically, such situations are often encountered in clock-distribution networks, which use thick and wide metal wires. These wires have low resistance and possibly exhibit significant inductive effects. Fig. 5 shows an example of these inductive effects. The lower resistivity interconnect exhibits overshoots and ringing because of the existence of inductance. However, typical timing-analysis tools utilize an RC-only interconnect model that assumes that the influence of inductance is negligible. When the inductive effect is significant, the accuracy of the timing analysis may thus be degraded. In general, a good indicator of the timing-estimation error between RC and RLC models is the damping factor of an RLC line or the ratio between the input-signal rise time to the time-of-flight of the signals across the line [27]. The damping factor ξ is given by

$$\xi = \frac{Rl}{2}\sqrt{\frac{C}{L}} \tag{1}$$

where R, L, and C are unit-length resistance, inductance, and capacitance, respectively, and l is the length of the line. If ξ increases, the inductive effects decreases, and the RC model becomes appropriate. On the other hand, the ratio between the rise time and the time-of-flight is given by

$$\frac{t_r}{2l\sqrt{LC}} \tag{2}$$

where t_r is the input rise time of the signal. The larger the ratio, the more appropriate the RC model becomes for an interconnect. Possible methodologies to control these values include the rules of repeater insertion for long interconnects, slew-rate control, and power/ground distribution design for inductance management [29]. Although most interconnects are insensible to on-chip inductance, it is useful to screen wires influenced by inductance at the interconnect-design phase [30] because the computational cost of on-chip inductance extraction and inductance-aware timing or noise analysis are quite high and immature yet.

In a SoC design, intellectual-property blocks for a radio-frequency (RF) interface are often embedded. To precisely characterize RF interconnects, substrate effects therefore have to be accounted for [31], [32]. However, a large number of filaments are required to express the skin and proximity effects by using a partial-element-equivalent-circuit (PEEC) model [33]. As a result, it is difficult for filament-based extractors to extract interconnect inductances and resistances both accurately and efficiently [34]. Several techniques to solve this problem have therefore been proposed [35].

C. Modeling of Dummy Fills

Irregular metal distribution increases the variation of metal thickness during CMP [36]. To assist planarization, dummy metal fills are inserted. The use of dummy fills introduces several issues: 1) ECO difficulty due to obstruction of dummy fills; 2) difficulty of keeping insertion uniformity; and 3) increased complexity in parasitic extraction. Algorithms for inserting dummy fills and feature patterns for achieving uniform interconnect capacitances have been devised to resolve these issues [11], [37]. Dummy fills are often inserted just before masks are manufactured rather than during the physical design of SoCs. This is because of the three issues stated earlier. To extract the parasitic capacitances from a layout with dummy fills, an enormous amount of processing time and memory space are required because of the existence of a large number of coupling capacitances.

A design that does not consider dummy fills may underestimate the influences of interconnect capacitance, delay, and crosstalk noise. Capacitance of a signal wire with dummy fills increases by 10%–35% in a metal-density range of about 20%–70% [38]. There are some methods that consider virtual dummy fills. A simple but effective modeling strategy is to ignore existing dummy fills by considering them as zero-width conductors. Fig. 6 shows a comparison of capacitance obtained

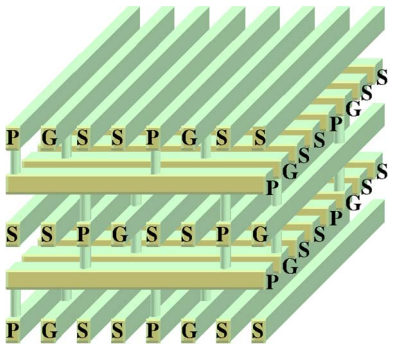

Fig. 7. Illustration of the dense power-ground interconnect architecture with a PGSS pattern.

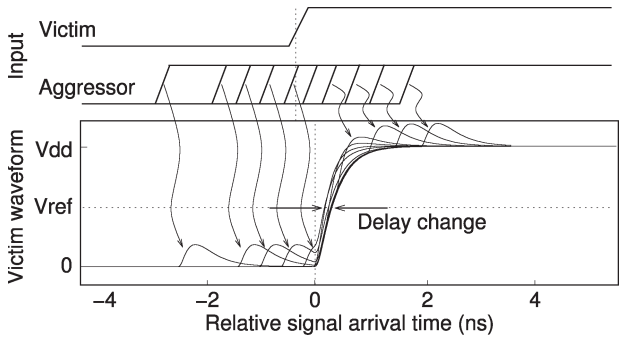

Fig. 8. Victim and aggressor signal-transition alignment and respective delay changes [45].

by the simple model with that obtained by measurement [38]. It is clear from the figure that the results from the simple model agree well with the measurement results. Another modeling strategy is to approximate the influence of dummy fills by calculating effective permittivity [37]. Higher accuracy can be obtained by formula-based approaches [39], [40]. For example, in [40], the number of structures for extraction that is reduced by a design of experiment is presented. Formula-based approaches are useful when real dummy fills (not virtual dummy fills) are placed in the physical layout during design phases.

D. Regular Interconnect Fabric

To improve manufacturability and extraction efficiency, regular interconnect fabric has been proposed [9], [10], [41], [42]. An example of regularly inserted power and ground interconnects is shown in Fig. 7 [43]. Regular fabric is expected to effectively reduce intradie interconnect variations. Moreover, the number of structures for parasitic extraction is significantly reduced. It also has beneficial effects regarding runtime, memory usage, size of interconnect library, and efficiency and accuracy of parasitic extraction. Compared with current cell-based designs, it have the drawbacks of increased signal delay, power consumption, crosstalk noise (for the wires without a ground wire), and chip area. However, the concept of regularity for metal wires is worth considering in the era of more advanced LSIs.

IV. Signal-Integrity Analysis

A. Capacitive Crosstalk Noise

Crosstalk noise is one of the most important effects of interconnect-related signal-integrity issues. In many design phases, careful and consistent attention is paid in avoiding crosstalk noise because it is a major source of deterministic timing variation. The effect of crosstalk noise can be divided into two: logic-state upset and timing failure. The former occurs when noise voltage on a victim net exceeds the logic-threshold voltage. If the inverted condition is propagated down to flip-flops (FFs), it causes a catastrophic error. Because of the preventive design flow with thorough verifications using modern EDA tools, wire routing is well controlled so that noise voltage does not exceed a logical threshold. The latter, which is equivalent to crosstalk-induced timing error, is the timing change due to crosstalk noise. It also causes a catastrophic error when false data due to the delay change is captured at downstream FFs. Fig. 8 conceptually shows the signal-timing change due to crosstalk noise. It is clear from the figure that the timing change occurs only when a timing overlap exists between the crosstalk noise and the victim signal transition. It is also clear that the amount of timing change depends on the relative timings of the aggressor and the victim wires [44], [45]. Even a small noise can cause an error if the victim net is on a critical path. The timing information of both the aggressor and victim paths is required to correctly analyze the effect of delay change [46]. Accordingly, delay-change analysis has to be much more comprehensive than the verification of the noise peak and tightly coupled with timing analysis.

B. Crosstalk-Noise Analysis

As the first step of crosstalk-noise analysis, analytical equations are widely used for pruning violation candidate nets used in crosstalk-noise verification tools [47]. The closed-form expressions for both noise-peak voltage and noise-induced delay have been proposed by limiting the interactions of the wires between two or three conductors. In [48], an intuitive expression for estimating noise peak voltage V_p between two geometrically identical wires is represented as

$$\frac{V_p}{V_{\rm dd}} \simeq \frac{1/2 + R_v/R_w}{1 + R_v/R_w} \frac{\eta}{1+\eta} = \frac{1/2 + R_v/R_w}{1 + R_v/R_w} \frac{C_c}{C_{\rm total}} \quad (3)$$

where $\eta = C_c/C_g$, C_c is the coupling capacitance between wires, C_g is the grounded capacitance of a wire, $C_{\rm total} = C_c + C_g$, R_v is the on-resistance of a victim-wire driver, R_w is wire resistance, and $V_{\rm dd}$ is the supply voltage. Other approximations for more general wire configurations are given in [15], [49]–[51], for example. These analytical equations are also used in placement and routing steps, where quick noise-shape evaluations are necessary. Multiple wire coupling can be considered by superimposing the analytical noise waveforms from different aggressors. The number of nets requiring the following detailed calculation in the crosstalk analysis can be further reduced by considering logical correlations and timing information.

The second step of the noise analysis includes more accurate, but time-consuming, analysis techniques such as linearized

circuit simulations using current-based models [52]. This step is much more difficult than one might think. Interconnects have a kind of *filtering effect* because of the low-pass nature of the RC parasitics. High-frequency components contained in a sharp noise will be rounded off when propagated along the long interconnections. Input–output transfer functions of logic cells also show nonlinear amplification characteristic as functions of both the magnitude and frequency components of the shape of an input voltage. This characteristic may prevent a narrow glitch from propagating down a signal path. Timing orthogonality of the arrival time of the glitch and the capture timing of the FF becomes other filter. When all these factors are simultaneously considered, the number of false positives is minimized.

C. Inductive Crosstalk

Electrical equivalent models for calculating the effect of inductive coupling noise are established, at least in principle. An example is the PEEC model, which introduces partial inductance in which a current return path is located infinitely far away. Although it is not difficult to construct parasitic models, including partial inductance, efficient use of the extracted models in a design flow is nontrivial. Given the far-reaching property of magnetic coupling, a significantly large number of wires have to be incorporated in a model than in the case of capacitive coupling. The resulting circuit matrix that has to be solved in the analysis becomes large and dense. It increases simulation time significantly, making it difficult to apply general wire configurations. To cope with this difficulty, matrix sparsification techniques such as [53]—utilizing the concept of inverted inductance matrix [35]—have been proposed.

Thus far, the effects of self- and mutual inductance are limited to the wires that are designed to have very low resistance. Examples are high-quality-factor inductors used in RF circuit designs, a long on-chip bus [54], [55], and global wires such as clock signals [56]. According to the criteria presented in the previous section, it is possible to judge whether a wire is dominated by inductance or not. In many SoC designs, wires are designed so that the on-chip inductance effect can be ignored.

D. Manufacturing and Design Considerations

Increase of wire density along with the advancement of technology scaling has been successfully facilitating high-density integration of functional devices on a chip. However, the reduction in wire dimensions adversely affects on-chip crosstalk because the accompanying increase in wire capacitance increases noise voltage and, thus, delay. These effects have to be alleviated by both process technologies and design methodologies.

From (3), selective use of low-k material as an interlayer dielectric material reduces crosstalk noise because it directly reduces coupling capacitance C_c. Reducing dielectric constant has numerous benefits in regard to circuit design, e.g., smaller delay and lower power consumption. However, given the physical limit of k, it is difficult to achieve significant reduction in capacitive crosstalk noise by developing low-k technology alone. Design approaches such as optimizing wire space or optimizing victim driver resistance R_v are therefore important.

In practical SoC designs, an even more difficult problem is the explosion of circuit size for signal-integrity analysis. As the process technology scales and complicated functionality is included in a chip, the number of wires to be considered for noise analysis increases exponentially according to Rent's rule [57]. In designs utilizing more advanced process technologies, major difficulties are caused by an overwhelming number of wires. For example, it is common that a back-annotated netlist for industrial designs exceeds a few gigabytes. In that case, one wire capacitance couples with those of many other wires. Even after the pruning, the number of aggressors is still significantly high. The corner-based estimations result in overestimation of the crosstalk noise to fix without area impact, which must be fixed without affecting the area of the chip. In these situations, statistical treatment of the noise analysis becomes important. To avoid overdesign, correct and consistent use of statistics is necessary. Pioneering work in [58] tried to estimate the effect of noise-induced delay early in the design stages so that designers can prevent their designs from suffering excessive noise-induced delay in the later design stages. Efficiently determining dominant aggressors to fix crosstalk-induced delay is another approach to cope with the design-size scaling [59].

Following the intuitions from analytical equations, EDA tools try to avoid or fix negative effects of crosstalk noise with a minimum penalty. There are several choices to achieve this objective: wire-space spreading, buffer insertion, aggressor downsizing, victim upsizing, and victim wire shielding. Naturally, different ways of fixing the effects have different effectiveness and overhead. Wire shielding, for example, almost completely eliminates lateral signal couplings but brings the penalty of doubled wire area. Wire-space spreading and buffer insertion are effective as compared to the area required for the modifications because coupling capacitance is inversely proportional to the number of inserted buffers n or wire spaces s. Making $n = 2$ or making space s twice the minimum space is much easier than cutting k by half. Reducing k is no doubt attractive but effective prevention and fixing by design are also indispensable.

Presently, interconnect signal integrity is considered in almost all design phases. Preventive design for signal integrity is now the key technology for achieving better timing convergence at the expense of a little overhead. Recently, timing is not a single objective, but its variability has to be definitely controlled and considered. At the same time, accurate noise estimation considering statistical properties of routed nets is important in assuring that signal integrity is considered in even earlier design phases such as signal-integrity-aware physical synthesis.

V. Timing Analysis

A. Waveform Propagation

CMOS combinational circuits consist of logic gates and interconnects, and they are connected alternately. STA

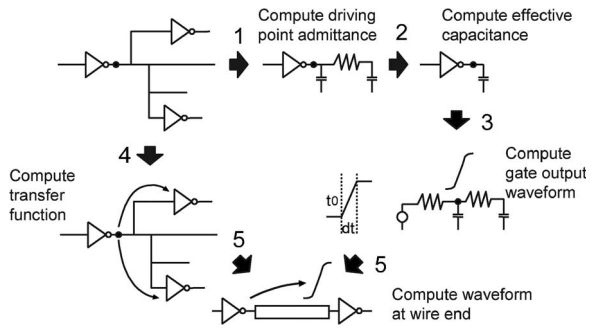

Fig. 9. Overview of waveform propagation.

computes propagation delays of logic gates and interconnects and derives the total circuit delay by propagating signal waveforms throughout a circuit. The sum of gate and interconnect propagation delays can be approximated as [48]

$$T_{50} = 0.4R_{\rm int}C_{\rm int} + 0.7R_{\rm int}C_L + 0.7R_{\rm tr}C_{\rm int} + 0.7R_{\rm tr}C_L \tag{4}$$

where $R_{\rm tr}$ is output resistance of a driving gate, $R_{\rm int}$ and $C_{\rm int}$ are interconnect resistance and capacitance, respectively, and C_L is input capacitance of the fan-out gate. In the case of process technologies where interconnect resistance is much lower than gate-output resistance, the first and second terms of (4) are small as compared to the other terms, and interconnects can be reasonably modeled as capacitance. In this case, the waveform at the gate output is identical to the waveform input at the fan-out gate. However, interconnect resistance is currently not ignorable; hence, the input waveform at the fan-out gate has to be computed separately from the output waveform at the driving gate.

Fig. 9 shows the current state-of-the-art STA, which comprises the following five steps.

1) Compute the driving point admittance of a driving gate and replace the interconnect load with an RC π load [60].
2) Derive an effective capacitance that makes the output waveform close to the actual output waveform with RC π load [61], [62], since characteristics of logic gates are generally characterized by assuming that the output load is purely capacitive in the timing/power library.
3) Compute the gate output waveform. A lookup table, which is constructed by precharacterization with SPICE, is often used for calculating the gate output waveform while considering nonlinear characteristics of MOS transistors. The input parameters are the slew of the input signal and load capacitance, and the output parameters vary according to the gate-delay models used. The accuracy of the computed output waveform thus also varies according to the gate-delay model used. Some representative models are the nonlinear delay model, the Thevenin equivalent-circuit model [63], and the industrial current-source models [64], [65].
4) Compute the transfer function for the interconnect. A high-order transfer function is approximated to a low-order function [29], [66].
5) Compute the waveform at the receiver end of the interconnect by using a reverse Laplace transform, which then becomes the input waveform at the fan-out gate. When the derived waveform shape is different from the shape assumed in the gate-delay model, the waveform is approximated [67].

Recently, to cope with various input-waveform shapes and output loads, current-source models, which model a gate with a current source and capacitances that are controlled by I/O voltages [52], [68], have been proposed. Waveforms at interconnects where the resistive effect and coupling noise are severe are computed by a simplified transient analysis with a current-source model for improving accuracy.

B. Timing Analysis for Variability

Manufacturing variability of transistors and interconnects, environmental fluctuation, and modeling error are categorized into the following five components.

Die-to-die component
: Variation of chip-average characteristics (including wafer-to-wafer and lot-to-lot variations).

Random component
: Component that originates from statistical fluctuation and cannot be fundamentally eliminated.

Spatially correlated component
: Gradual variation within a chip.

Position-dependent component
: Variation component determined by coordinates in a wafer and dependent on characteristics of manufacturing equipment.

Layout-dependent component
: Deterministic variation depending on layout shapes and density.

Strictly speaking, the layout-dependent component is expected to be modeled; however, when modeling cost is high, it is approximately treated as a random or spatially correlated component.

In regard to interconnect variation, die-to-die variation due to layer-thickness variation, layout-dependent and position-dependent components mainly attributed to CMP and lithography processes, and extraction errors of interconnect resistance and capacitance are thought to be dominant. To improve modeling accuracy, RC extraction by CMP simulator has been proposed [12]. The random component due to line edge roughness [5] is thought to be negligible because interconnect wire width or length is much larger than the size of gate poly, and the random component is averaged out. Reference [69] reports that the capacitance-extraction error of industrial state-of-the-art tools is $\sigma = 1.5\%{-}5\%$.

1) Corner-based Analysis: Corner-based analysis, which verifies timing specifications at fast, slow, and other process and environmental corners, has been widely adopted to take die-to-die variation into consideration. So far, die-to-die variation has been larger than within-die variation (including random and spatially correlated components), so corner-based analysis has been used for sign-off verification.

On the other hand, identifying interconnect corners is difficult. The best and worst corners of interconnect structural

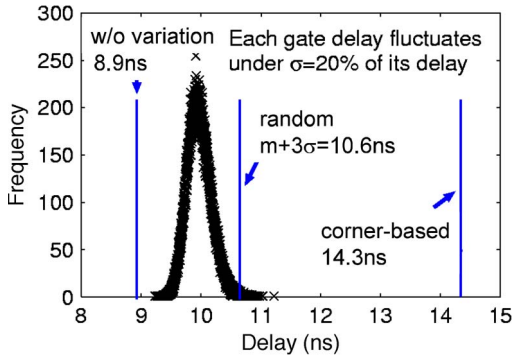

Fig. 10. Example of timing-analysis result under process variation.

parameters vary according to the relative dominance of each term in (4) [70]. As an example, it is supposed that spacing becomes larger and interconnects become narrower. In this case, interconnect resistance increases and capacitance decreases. When the third term in (4) is dominant, the delay decreases. In contrast, when the second term is dominant, the delay increases. Moreover, when the first term is dominant, the delay increase or decrease depends on the balance of increase in resistance and decrease in capacitance. This means that the best and worst corners are different instance by instance, and universal corners cannot be defined. To overcome this problem, the worst cases for capacitance, for RC product, and for resistance are derived, and all of them are usually used in sign-off timing verification. Reference [71] experimentally showed that there are three best/worst structures according to the wiring situations.

In addition, LSIs under many operating conditions, e.g., supply voltage, substrate bias, and clock frequency, are becoming commonplace, and timing verification under every operating condition is required before fabrication of such LSIs. Under some configurations of supply and threshold voltages, the worst case for transistor on-current exists at low temperature [72]; thus, the corner must be carefully defined particularly in VLSI with dynamic voltage scaling. Under all possible corner conditions (transistor, interconnect, temperature, and supply voltage) and all operational modes (such as normal and scan-test mode), timing specification has to be verified. The STA for multicorners and multimodes increases required CPU time drastically. To improve the efficiency of STA, [73] proposes a technique that analyzes timing at multiple corners simultaneously, and [74] presents a gate-delay model that can cover a wide range of manufacturing and environmental variations with small additional characterization cost.

2) Statistical analysis: Excessive overdesign due to corner-based analysis has been regarded as a problem because within-die variation has become comparable to or dominant over die-to-die variation. Fig. 10 shows an example of the result of timing analysis on a small combinational circuit. Three sets of results are plotted under the following three assumptions: All variations consist of die-to-die components, all variations are composed of random components, and no variation exists. It is clear that when a random component is dominant, corner-based analysis (which misinterprets all variation as die-to-die components) gives a pessimistic result. In reality, there are both random and die-to-die components, and an intermediate distribution will be observed. To accurately estimate the delay distribution, the correlations between variation sources must be obtained, and then, decomposition of variation components is essential.

Given the background aforementioned, SSTA, which assumes that the delay of each element is given as a probability density function, for estimating the maximum circuit delay statistically has been intensively studied. In the early stages of research, potential importance of SSTA has been discussed under the assumption that delay distributions are Gaussian and uncorrelated [17]. Subsequently, how to consider spatially correlated components and correlation of reconvergent paths have been researched, and an analysis method that rigidly computes correlation coefficients of Gaussian random variables in SSTA was proposed [19]. Furthermore, to analyze larger circuits, more efficient treatment of this correlation was investigated. Reference [20] proposes that spatially correlated components are converted into a set of uncorrelated variables (principal components) by using principal-component analysis (PCA), which drastically facilitates the consideration of correlation in SSTA. Recently, ways on how to consider a non-Gaussian distribution [16] and environmental fluctuation [75] have been explored. In SSTA, delay variation of each gate and interconnect is often expressed using sensitivities to variation variables by first-order Taylor expansion. Element delay d is expressed as

$$d = \mu_d + \sum_{p_i} \left[\frac{\partial f}{\partial p_i}\right]_0 \Delta p_i \tag{5}$$

where p_i is the ith variation variable and μ_d is the average of d. $[\partial f/\partial p_i]_0$ is the sensitivity of element delay to p_i, and Δp_i is the shift of p_i from its average.

When correlated variables are orthogonized by PCA, Δp_i is expressed as a linear summation of principal components. Thus, with (5), d can be expressed as a linear summation of principal components. Adding a random component, within-die delay variation is usually represented as

$$d = \mu_d + \sum_{i=1}^{n} k_i p_i' + N\left(0, \sigma_{\mathrm{rnd}}^2\right) \tag{6}$$

where n is the number of principal components, p_i' is the ith principal component, k_i is the sensitivity of delay to p_i', and σ_{rnd} is the standard deviation of random component.

Computation of signal arrival time requires sum and max operations, which are primitive operations in STA. When delay d and signal arrival time are expressed in (6), their sum is naturally expressed in the form of (6), by just adding average values, coefficients of each principal component, and variances of random component. On the other hand, the max operation is not straightforward, since it is a nonlinear operation. Even when a_1 and a_2 are Gaussian, $\max(a_1, a_2)$ is no longer Gaussian. For this problem, Clark [76] derived closed-form expressions of the average and variance of $\max(a_1, a_2)$. By approximating $\max(a_1, a_2)$ to a Gaussian distribution using the closed-form expressions, the result of the max operation of two signal

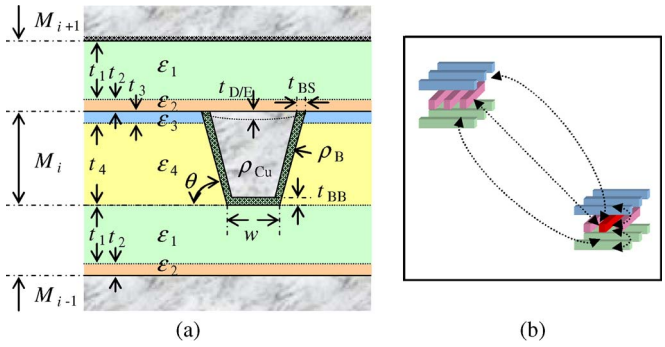

Fig. 11. Interconnect informational examples. (a) Cross-sectional parameters. (b) Within-die spatial correlations.

arrival times can be expressed in the form of (6) [20]. In this case, covariance of two arrival times expressed in (6) can be easily computed, since the correlation coefficient between p'_i and $p'_j (i \neq j)$ is zero.

Interconnect delay can be efficiently handled in SSTA using (5). When Elmore delay is used, deriving sensitivities to physical interconnect parameters is not very difficult; however, when model order reduction (MOR) is used for interconnect-delay analysis, which is described in Section V-A, the computational time needed for sensitivity derivation becomes a problem. To solve this problem, MOR (which accepts parameter variation) has been studied [77]. On the other hand, in the case that within-die interconnect variation is much smaller than within-die transistor variation, it might be possible to consider die-to-die interconnect variation only and ignore within-die interconnect variation. We have to carefully consider the required accuracy of timing analysis and examine the scaling trend of variability.

VI. Future Perspective on Interconnect Modeling

As stated in the previous sections, interaction between design and manufacturing has become a requisite, at least superficially. We expect this trend to become much more commonplace and essential in regard to the LSI designs that utilize future process technologies. In this section, we summarize a wish list of the necessary interactions and then revisit the future roles of design technology, which hopefully facilitate the high-performance and cost-effective LSI designs.

A. Wish List for Design Technology and Manufacturing Interaction

Our wish list simply covers two key points: continuous technology innovation and accurate variability representation. The former is, of course, closely related to minimizing process variations. An interconnect technology with low-k dielectrics and low-resistivity interconnects is necessary to realize high-speed and low-power SoCs. The latter is related in guaranteeing proper operation of a designed chip. As stated in Section II, the key is the accuracy of variation information (on which design methodologies fully rely). In designing an LSI with more advanced technologies to improve design accuracy, quality, yield, cost, even higher accuracy will be essential.

An example of interconnect information is shown in Fig. 11. Fig. 11(a) shows a cross section of an interconnect with material property and geometrical information. In this paper, M is the metal layer, w is bottom interconnect width, t is thickness, θ is the angle of an inverse trapezoid, ρ is resistivity, and ϵ is the dielectric constant. The nominal values and the standard deviations representing inter- and intradie variations of each dimension are the basis. Correlations between the parameters are also required if parameters are not independently distributed. Changes in temperature- and frequency-dependent parameters also have to be estimated. Furthermore, in the cases that the variation parameters have the location dependence, those information should be also utilized in design tools. Although the example shown in Fig. 11(a) is for a wire profile, similar information for all metal and insulator layers, including a via structure, is required. Variation of via resistance has a significant impact on interconnect delay; thus, accuracy of its measurement is vital.

Fig. 11(b) shows spatial correlations between interconnects. Arrows shown in the figure represent correlations between the middle interconnect of the structure on the bottom and the other interconnects. These correlations help EDA tools to narrow down the range of variations in other metal layers once the variation of one layer is known. Clarifying the correlation between distance, position, and layers can be useful to build high-quality libraries that enable design of smaller chips with lower cost. On the other hand, the lack of correlation information in general leads to overdesign.

In addition, accurate information concerning reliability has become very important. Faulty chips due to the earlier-stated variability must be removed in the testing process after fabrication. However, time-dependent reliability issues—which are difficult to filter in testing—are more serious. A representative reliability issue concerning interconnects is EM. In design verification, in general, EM checking is conducted by referencing the current-density limitation in an EM design rule and comparing it with the calculated average current of the target interconnect. However, the influence of a maximum instantaneous current is unclear and unchecked in most designs. Similarly, the "via–void" problem, in particular, due to SM, is becoming crucial in industrial designs; thus, more accurate information is required. As for DFM/DFY, we need detailed information describing what type of reliability issues, at what spots, in what conditions, and to what quantitative extent do interconnect wire/via patterns become risky. Once their information is provided, design tools can include them as part of a cost function for design objectives.

It may be difficult to provide a lot of information because physical measurement such as SEM and TEM demands an enormous amount of time and high cost. Technical developments for simplifying, for example, the extensive use of *in situ* electrical measurements will thus become more important (as touched on in Section III-A).

B. Roles of Design Technology

Efficient design flow is extremely important for the differentiation of products, particularly when many competing

companies share jointly operated fabrication lines or utilize the same foundry services. It is the design flow that differentiates quality, design time, chip size, and reliability. Only an innovative design technology can yield large profits in regard to SoC products. In that sense, the roles of design-technology engineers—who interface between the manufacturing process and design process—gain more importance. The variability and reliability issues described earlier can be dealt with in circuit designs with the provided information. For example, delay variation caused by interconnect variation can be correctly handled and even compensated by the SSTA tools described in Section V. Even so, extraction and analysis methods have to be changed accordingly to achieve enhanced accuracy. Moreover, via–void issues due to SM and EM may be at least partially avoided in design by adding extra via(s) to truly risky spots by, for example, changing routing or inserting buffers. The most important point regarding addressing this issue is the collaboration. Such collaboration by understanding what can be or cannot be done both from the process-technology side and the design-methodology side is the key practice for realizing effective successful design.

The following lists examples of information needed for clarifying the target of technology developments on the manufacturing side.

1) What blocks of SoC are susceptible to interconnect wire/via variability?
2) What is the range of interconnect variability for different blocks such as memories, analog circuits, and random logics?
3) For circuit operation, what is the critical limitation, which cannot be evaded by design techniques, on variation of each parameter for interconnect wires and vias?
4) How much is incremental design cost with increase in interconnect variability?
5) How much is design cost for DFM/DFY such as redundant via insertion?
6) How beneficial are low-k and low resistivity in designs and the product market?

These parameters may become requests sent to the design side from the manufacturing side, and they are useful for manufacture for designability—which is complementary to the idea of DFM. Finding optimal solutions of technology developments in both sides is crucially important.

Examples of future design-technology developments are listed as follows.

1) Minimizing chip cost: Chip-size-minimization techniques used in floorplanning, optimization of pad number and assignment, routing, and logic-cell design.
2) Improving the yield of chips per wafer: DFY techniques based on more detailed manufacturing information.
3) Improving analysis accuracy: Realistic statistical-analysis methods based on more detailed and physically accurate information.
4) Exploiting variability: Design techniques for making good use of variability rather than trying to cancel variability.
5) Eradication of defective products on the market: Design techniques for reliability, including statistical test methods for robust quality warranty.
6) Cope with more complicated and larger scaled interconnects: Efficient modeling and analysis techniques, including statistical MOR.
7) Reducing ECO iterations and design time: Proactive techniques, for example, on-the-fly IR-drop, EM, crosstalk, and timing analyses during placement.
8) Maximize chip performance: Post silicon tuning to compensate negative effect of variations.

In summary, primary points in regard to future developments of design technology will be variation-, yield-, and reliability-aware design for maximizing profits of SoC products.

VII. Conclusion

In this paper, the importance of interconnect modeling in an advanced SoC design flow was described first. Recent interconnect-modeling techniques were then reviewed. Finally, requests to the manufacturing side in view of the design side were discussed, and the importance and perspective of design technology were described. As technology scaling advances, accurate information of interconnect variability and reliability is becoming ever more important in regard to improving accuracy, quality, yield, and cost concerning SoC designs. For maximizing the profits of products, closer collaboration between the manufacturing and design sides is essential. We hope that this paper will be helpful for the development of future technology from the viewpoint of both manufacturing and design.

Acknowledgment

The authors would like to thank K. Oya, Y. Takashima, and T. Watanabe (who are designers of advanced SoC products) for their valuable comments.

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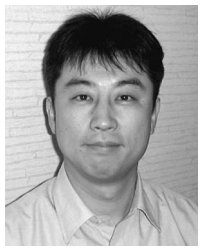

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