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Performance Limitation of On-Chip Global Interconnects for High-Speed Signaling

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SUMMARY This paper discusses performance limitation of on-chip interconnects. On-chip global interconnects are considered to be a bottleneck of high-performance LSIs. To overcome this issue, high-speed signaling and large throughput interconnection using electrical wires have been studied. However the limitation of on-chip interconnects has not been examined sufficiently. This paper reveals the maximum performance of on-chip global interconnects based on derived analytic expressions and detailed circuit simulation. We derive trade-off curves among bit rate, interconnect length, and eye opening both for single-end and for differential signaling. The results show that differential signaling improves signaling performance several times compared with conventional single-end signaling, and demonstrate that 80 Gbps differential signaling on 10 mm interconnects is promising.

key words: *global interconnect, high-speed signaling, performance limitation*

1. Introduction

Advances in LSI fabrication technology accelerate the continued increase of operating frequency. A clock frequency is expected to exceed 15 GHz in 2010 [1]. A big challenge in this era is high-speed and large capacity signal transmission. Recently to attack this problem, high-speed signaling and throughput driven interconnection are becoming a hot research topic both in design and EDA communities [2]. Optical communication instead of metal wire signaling is also studied [3].

The current signaling scheme is roughly classified into single-end and differential signaling. Differential signaling is used for on-chip high-speed and long-distance interconnection as well as off-chip signaling, for example clock distribution [4]. On the other hand, single-end signaling is very common in chip design. Each scheme has both advantages and disadvantages, and hence circuit designer should be aware of the maximum performance of both signaling schemes, and know in what situation differential signaling is preferable, or rather a sole solution.

Reference [5] proposed an analytical expression of the limitation of electrical interconnects at various levels such as on-chip, on-board, and cables. It reports that the limitation of on-chip interconnect is about 30 Gbps for terminated single-end transmission. However, a conventional on-chip single-end signaling has an open-end termination because of a small input capacitance of a CMOS receiver. Also, we should examine the performance of differential signaling. Another issue to be discussed is the effect of crosstalks and interconnect dispersion which are not considered in the analysis of Ref. [5].

In this paper, the performance limit of on-chip interconnects is discussed. There are several factors that degrade signal integrity, i.e. attenuation, crosstalk and dispersion. Experimental results show that the main factor that inhibits high-speed signaling is attenuation in crosstalk-controlled interconnect structures. From the viewpoint of attenuation, we analytically derive the maximum eye opening in voltage for open-ended single-end signaling, terminated single-end signaling and differential signaling. Experimental results by circuit simulation verify that the analytical performance estimation is valid even when crosstalk noise and frequency-dependence of interconnects are considered. The analytic estimation provides trade-off curves among bit rate, length and eye opening. They indicate the performance difference between single-end and differential signaling and reveal in which region differential signaling has a significant advantage over single-end signaling. We observe that the performance limitation depends on the receiver performance. The improvement of the receiver sensitivity makes differential signaling achieve tens Gbps signaling on the interconnects with the length up to several centimeters.

In Sect. 2, we derive expressions for analytical performance estimation. We experimentally verify the analytical expression in Sect. 3, and Sect. 4 discusses performance trade-off curves of signaling. Section 5 concludes this paper.

2. Analytical Estimation of Interconnect Performance

This section derives analytic expressions that estimate the performance of on-chip global interconnects. We here focus on attenuation characteristics as the most dominant factor that prevents global signaling, and perform an analytical performance estimation based on simplified interconnect and waveform models. The effect of crosstalk noise and dispersion is examined in Sect. 3, which confirm that the simplified model based on the attenuation is valid for on-chip interconnects.

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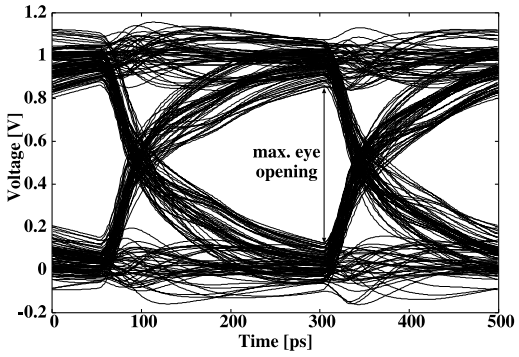

Fig. 1 An example of eye-diagram and the figure of merit.

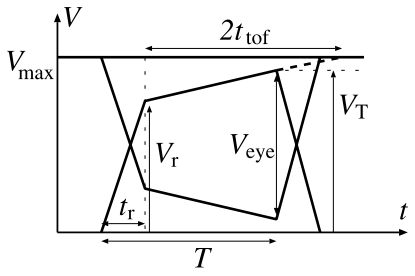

Fig. 2 Piecewise linear waveform model.

2.1 Figure of Merit for Signaling Performance

Eye-diagram is commonly used to evaluate the feasibility and quality, which include bit error rate, of signaling systems [6]. Figure 1 shows an example of eye-diagram. Large eye opening area means that signaling has timing/noise margin. To evaluate the area of eye opening, rectangle/hexagon eye mask is used commonly. However, for simplify in this paper, we use the maximum eye opening in voltage shown in Fig. 1 as a figure of merit. In the case of on-chip signaling, attenuation is the most important factor that limits high-speed long-distance signaling. In this condition, the eye opening in time is strongly correlated with that in voltage, and hence we discuss the performance limitation by evaluating the maximum eye opening in voltage.

2.2 Analytical Performance Estimation

We here describe analytical performance expressions that estimate the maximum performance of interconnects.

2.2.1 Assumptions on Derivation

We explain three assumptions used for the derivation of the analytic expressions.

The first assumption is that the interconnect structure is designed to reduce crosstalk noise. Although crosstalk noise affects eye-diagram, it can be suppressed in a well-designed interconnect structure by shielding and spacing. In Sect. 3, we experimentally verify that the effect of crosstalk noise can be controlled by the interconnect structure and the attenuation is the dominant factor which degrades the eye-opening. We also neglect the effect of waveform dispersion. Interconnect characteristics is frequency dependent because of skin- and proximity-effect and return-current distribution, which causes waveform dispersion. However the effect of waveform dispersion is small compared to that of the attenuation. In the analytical estimation, crosstalk and dispersion are not considered.

The second assumption is involved in impedance-matching. When driving transmission-lines, an impedance-matched driver is the optimum solution [7]. In this paper, we assume that the impedance-matching is achieved. For conventional single-end signaling, the near-end is driven by a matched driver and the far-end is open-ended, because the far-end is terminated by a small input capacitance of the receiver. To examine the effect of the termination, the single-end signaling with impedance-matched termination is also evaluated. For differential signaling, the near-end is the same as the single-end signaling. The far-end of the differential pair is terminated by a bridge termination. The bridge termination is commonly used in Low-Voltage-Differential-Signaling (LVDS).

The third assumption is that the waveform at the far-end is expressed as a piecewise linear expression as shown in Fig. 2. T is the minimum period of input pulse. t_{r} is the signal transition time of waveform at the far-end, and we assume that t_{r} is equal to the transition time of input pulse. This assumption is valid when distortion due to frequency-dependence of transmission-line characteristics is weak. $V_{\max}$ is the voltage amplitude when the input value is continuously "1." In the case of open-ended transmission-lines, $V_{\max}$ is equal to the supply voltage. As for terminated transmission-lines, $V_{\max}$ is determined by the resistance of the termination of each end and the DC resistance of the interconnect. At the near-end, the half amplitude of input pulse is injected by the impedance-matched driver. As the injected voltage wave travels on the interconnect, the amplitude decreases by attenuation. The voltage V_{r} means the rise voltage at the far-end of the interconnect. On open-ended transmission-lines, V_{r} is the twice of the amplitude of the arrival voltage wave because of perfect reflection. V_{r} is determined by the attenuation of the interconnect. On lossy transmission-lines, the voltage continuously rises from V_{r} [8]. V_{T} is defined as the voltage after the time T passed since the signal transition started. From a closed-form expression of waveform on lossy transmission-lines, Ref. [9] shows that the voltage at the far-end reaches $V_{\max}$ after the time $2t_{\mathrm{tof}}$ passed when the interconnect is driven by a matched driver. The time t_{tof} is the signal time of flight and $t_{\mathrm{tof}} = l/v$, where l is the interconnect length and v is the velocity of the propagating wave. Therefore V_{T} is determined from V_{r}, $V_{\max}$ and t_{tof}, which provides simple yet efficient expressions of eye opening shown in the next paragraph.

2.2.2 Eye-Opening Derivation

We derive an equation that represents the maximum eye opening. We set, in this paper, that the supply voltage is 1, without losing generality, because the target circuit is linear.

From Fig. 2 and the discussion in the previous section, the maximum eye opening voltage $V_{\rm eye}$ is expressed by

$$V_{\rm eye} = \begin{cases} V_{\rm max} - 2(V_{\rm max} - V_{\rm T}) = 2V_{\rm T} - V_{\rm max} & (T < 2t_{\rm tof}) \\ V_{\rm max} & (T > 2t_{\rm tof}) \end{cases}. \tag{1}$$

The maximum voltage $V_{\rm max}$ is expressed as

$$V_{\rm max} = \frac{Z_{\rm term}}{Z_{\rm driver} + R_{\rm line} + Z_{\rm term}}, \tag{2}$$

where $Z_{\rm driver}$ is the driver output impedance, $Z_{\rm term}$ is the terminal impedance and $R_{\rm line}$ is the DC resistance of the interconnect. As mentioned before, we assume $Z_{\rm driver}$ is equal to the characteristic impedance Z_0. The rise voltage $V_{\rm r}$ depends on the attenuation of the interconnect and the reflection coefficient at the far-end of the interconnect. We define an attenuation parameter n as $n = {\rm e}^{-\alpha l}$ where α is the attenuation constant. Using the attenuation parameter n, the voltage $V_{\rm r}$ is expressed as

$$V_{\rm r} = (1 + \Gamma)\frac{n}{2}, \tag{3}$$

where Γ is the reflection coefficient at the far-end of the interconnect. From the piecewise linear assumption, the voltage $V_{\rm T}$ is expressed as

$$V_{\rm T} = \left\{ \frac{V_{\rm max} - V_{\rm r}}{2t_{\rm tof}}(T - t_{\rm r}) + V_{\rm r} \right\}. \tag{4}$$

2.2.3 Detailed Expressions for On-Chip Interconnects

In the previous section, we derive the equations in a general form. We show the equations specialized for some typical conditions of on-chip interconnects, that is, open-ended transmission-line, terminated transmission-line and terminated differential transmission-lines.

i. Open-ended single-end signaling

On open-ended transmission-lines, the terminal impedance $Z_{\rm term}$ is infinity. Therefore the maximum voltage $V_{\rm max}$ is equal to the supply voltage, which is equal to 1 in this paper. Because $Z_{\rm term}$ is infinity, the reflection coefficient Γ is equal to 1. So the rise voltage $V_{\rm r}$ is equal to n. The eye opening $V_{\rm eye}$ is expressed as

$$V_{\rm eye} = \begin{cases} \frac{1-n}{l/v}(T - t_{\rm r}) + 2n - 1 & (T < 2t_{\rm tof}) \\ V_{\rm max} = 1 & (T > 2t_{\rm tof}) \end{cases}. \tag{5}$$

The derived expression indicates that the maximum eye opening $V_{\rm eye}$ is determined by the minimum period T, the rise time $t_{\rm r}$, interconnect length l and the attenuation parameter n. The velocity v is determined by the dielectric constant of metal insulator.

ii. Terminated single-end signaling

On the terminated transmission-lines, $Z_{\rm term}$ is equal to Z_0. Therefore the reflection coefficient Γ is 0, and the rise voltage $V_{\rm r}$ is equal to $n/2$. Here the attenuation parameter n is approximately expressed as follows [8]

$$n = \exp(-\alpha l) \simeq \exp\left(-\frac{R_{\rm line}}{2}\sqrt{\frac{C}{L}}\right) \simeq \exp\left(-\frac{R_{\rm line}}{2Z_0}\right). \tag{6}$$

Equation (2) can be rewritten as

$$V_{\rm max} = \frac{Z_0}{2Z_0 - 2Z_0 \log n} = \frac{1}{2\,(1 - \log n)}. \tag{7}$$

From the difference of $V_{\rm r}$ and $V_{\rm max}$, the maximum eye opening is expressed as

$$V_{\rm eye} = \begin{cases} \frac{\frac{1}{2(1-\log n)} - \frac{n}{2}}{l/v}(T - t_{\rm r}) + n - \frac{1}{2(1-\log n)} & (T < 2t_{\rm tof}) \\ \frac{1}{2(1-\log n)} & (T > 2t_{\rm tof}) \end{cases}. \tag{8}$$

iii. Differential signaling

In the case of differential signaling, the expression of the eye opening $V_{\rm eye}$ is simply the twice of Eq. (8).

$$V_{\rm eye} = \begin{cases} \frac{\frac{1}{1-\log n} - n}{l/v}(T - t_{\rm r}) + 2n - \frac{1}{(1-\log n)} & (T < 2t_{\rm tof}) \\ \frac{1}{1-\log n} & (T > 2t_{\rm tof}) \end{cases}. \tag{9}$$

Please note that the attenuation constant of differential signaling is different from that of single-end signaling even if the interconnect structure is the same. This is because we have to use the interconnect characteristic for differential mode when evaluating the differential signaling. Therefore the resistance $R_{\rm line}$ and characteristic impedance Z_0 of Eq. (6) are different. In differential signaling, one signal wire of the pair becomes the current return path of the other wire. The return current is tightly confined, and hence the loop resistance of the differential pair is larger than that of single-end signaling and the loop inductance of differential pair is smaller than that of single-end signaling. The capacitance of differential signaling is larger than that of single-end signaling because the voltage of each wire transits to opposite direction. From Eq. (6), the attenuation parameter n of differential signaling is smaller than that of single-end signaling.

3. Verification of Analytical Estimation

In this section, we show some experimental results and demonstrate the validity of the analytical formulae in the previous section by detailed circuit simulation that considers crosstalk and dispersion as well as attenuation. We first

explain the conditions of circuit simulation. Next the simulation results and analytical estimation are shown such that the analytical estimation is verified.

3.1 Simulation Setup

We evaluate the eye opening by circuit simulation. First, interconnect R(f)L(f)C are extracted by 2D field-solver, because inductance of a long interconnect such as 10 mm is proportional to the length. The shunt conductance is negligible in LSIs because the electric loss of insulator is small. Figure 3 shows the interconnect structure which corresponds to a bus structure for long-distance signaling. We assume a 45 nm process in Roadmap [1]. In Fig. 3, M10 means the tenth metal layer and we assume M11 and M12 are the special thick layer for long distance interconnect or power/ground wire. In M12, there are seven signal line ("S" in Fig. 3) and ten ground wires ("G" in Fig. 3). There are twenty ground wires in M10. In M12 layer, 4 μm width signal interconnects are aligned and shielding ground wires are allocated at every seven signal wires. The ground wires in the lower layers also affect the characteristics of the signal wires. Therefore the ground wires in M10 layer are taken into consideration. In M11 layer, there are some orthogonal interconnects. We assume that the interconnects in M11 have the same width and pitch as those in M12. Orthogonal interconnects affect to the capacitance and it does not affect to the resistance and the inductance. The interconnect characteristics are modeled by a frequency dependent coupled transmission-line model [10] implemented in a circuit simulator [11].

Figure 4 shows the experimental circuit. Each signal wire is excited by an ideal voltage source with an ideal resistance. The input pulses of signal wires are random non-return-zero patterns that are independent of each other. The pulse shape is trapezoidal with pulse period T and transition time $T/10$. In following section, we define "bit rate" by $1/T$. For simplicity, the supply voltage is 1 V, because of the linearity of the circuit model. We evaluate the eye opening of each signaling scheme with various pulse period T and interconnect length l.

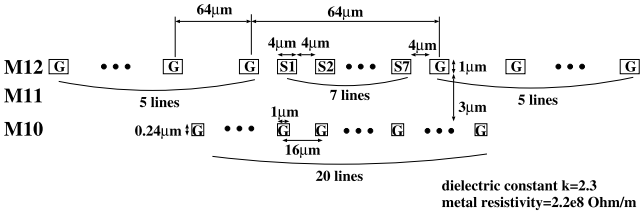

Fig. 3 Cross section of the interconnect.

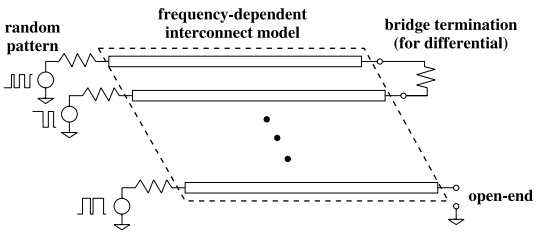

Fig. 4 Experimental circuit.

3.2 The Effect of Attenuation and Crosstalk Noise

Our analytical model focuses the attenuation of the interconnects and ignores the other factors, such as crosstalk noise and dispersion. The crosstalk noise if exists, disturbs the waveform and it can be the limiting factor of the interconnect performance. We discuss the effect of the attenuation and the crosstalk noise for the performance degradation.

Figure 5 shows the bit rate vs. eye-opening curves on several crosstalk noise conditions. The line labeled "7 signal lines" shows the simulation result when 7 wires in Fig. 3 are driven independently. This result corresponds to the performance under the strong crosstalk noise. The line labeled "spacing" is the result when the signal lines S1, S3, S5 and S7 are removed. In other words, the spacing between signal lines is enlarged by 3 times. The line labeled "shielding" is the result when the signal lines S1, S3, S5 and S7 are grounded. This means that each signal wire has shield wires on both side. The line labeled "w/o crosstalk" means that the only one signal line is excited and the other lines are quiet. From Fig. 5, the eye-diagram of "7 signal lines" is degraded and the curve is far from the curve of analytical estimation. However, crosstalk noise can be eliminated by the spacing or the shielding. As shown in Fig. 5, the result of "shielding" is almost the same as that of "w/o crosstalk" and that of "formula." This means that the effect of crosstalk noise is small if the interconnect is well-designed against the crosstalk.

On the other hand, the attenuation of the interconnects cannot be eliminated. Figure 6 shows the attenuation constant as a function of interconnect width for co-planar and micro-strip structures. The attenuation constant is a decreasing function with respect to interconnect width. However, it is seen that the decrease is quickly saturate and it does not decrease to a small value even if we use fat wires for the signal line, since skin and proximity effects force the current to concentrate near the surface of the signal and ground

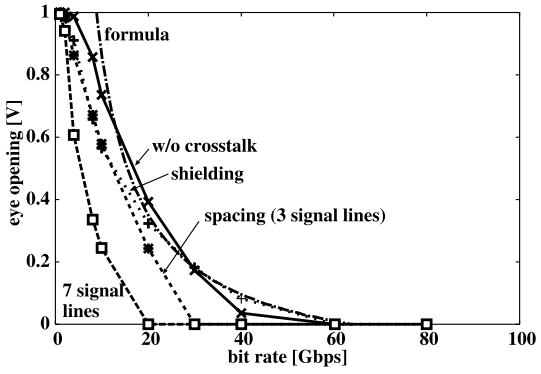

Fig. 5 The effect of crosstalk noise over the eye-opening.

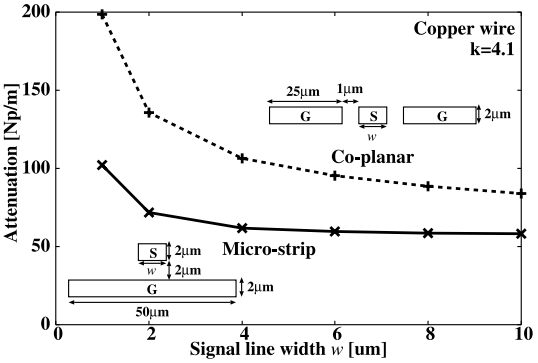

Fig. 6 The attenuation vs. interconnect width (at 10 GHz).

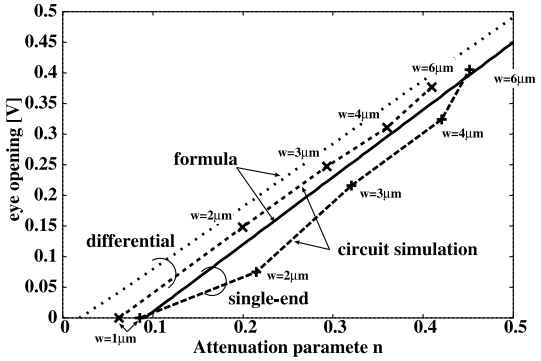

Fig. 8 Attenuation vs. eye opening (at 20 Gbps).

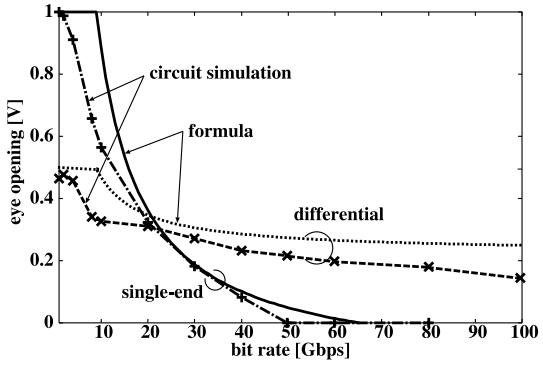

Fig. 7 Bit rate vs. eye opening.

interconnects that face each other. From above discussion, the attenuation is the dominant factor in the estimation of the performance limitation. Therefore in the following sections, we discuss the crosstalk-controlled interconnects structure with attenuation.

3.3 Bit Rate vs. Eye Opening Voltage

We show the bit rate versus the maximum eye opening. Figure 7 shows the analytical estimation and the simulation results. The interconnect structure is Fig. 3. To evaluate differential signaling, two signal wires are driven by differential signal and other 5 signal wires are driven by random pattern, which simulates the worst condition of a differential signaling embedded in a single-ended environment. In the case of single-end signaling, S1, S3, S5 and S7 wires are replaced with ground wires, which means that each signal wire has shield wires on both side. In this case, the interconnect resource used by single-end signaling and that used by differential signaling become the same. The far-end of interconnects are open-ended. From Sect. 2, the eye opening of terminated single-end transmission-lines are the half of differential signaling. So we compare the open-ended single-end signaling and differential signaling. The interconnect length is 10 mm and the attenuation parameter of single-end signaling is $n = 0.42$, that of differential is $n = 0.36$. These attenuation parameters are calculated at the representative frequency proposed in Ref. [12]. The representative frequency is decided by the interconnect length. In this case, the representative frequency is 5 GHz. In Fig. 7, analytical estimation (labeled "formula") are valid because it is close to the experimental results (labeled "circuit simulation"). Figure 7 shows that in low bit rate region up to 20 Gbps, the eye opening of single-end signaling is larger than that of differential signaling. This is because $V_{\max}$ of single-end signaling is large. However as the bit rate becomes higher, the eye opening of single-end decreases very rapidly and becomes almost 0 over 40 Gbps. This is because $V_{\max} - V_{\mathrm{r}}$ of single-end becomes larger by attenuation.

From Fig. 7, the discrepancy between the analytical estimation and the circuit simulation becomes larger as the bit rate becomes higher. In differential signaling, the difference is about 30% at 80 Gbps and about 50% at 100 Gbps, since the effect of waveform dispersion is not negligible at such high bit rate. Therefore the applicability of the analytical estimation has a limitation with respect to the bit rate. For example, from Fig. 7, the coverage of the analytical estimation becomes up to to 80 Gbps if we limit the maximum error below 30%.

3.4 Attenuation vs. Eye Opening Voltage

Next, we examine the effect of attenuation for eye opening. We change the attenuation by setting different values to the width and spacing of the interconnect structure shown in Fig. 3. We use the same value for width and spacing from 1 μm to 6 μm in each configuration. Figure 8 shows the amount of eye opening as a function of the attenuation. Except the width and spacing of the interconnects, simulation set-up is the same as that of Sect. 3.3 at the signaling rate of 20 Gbps. As seen from Fig. 8, the maximum discrepancy is 0.07 V. The analytical estimation (labeled "formula") gives a good prediction of eye-opening under different attenuation values with different interconnect width and spacing.

4. Trade-off Curve of On-Chip Interconnects

By using the analytical performance estimation, we can obtain the trade-off curves of the interconnects. In this section, we show the performance tradeoffs among signaling scheme, bit rate, interconnect length and attenuation.

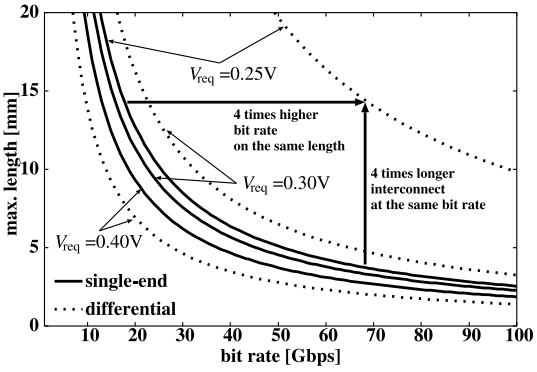

Fig. 9 Bit rate vs. maximum interconnect length with various receiver sensitivity (V_{req}).

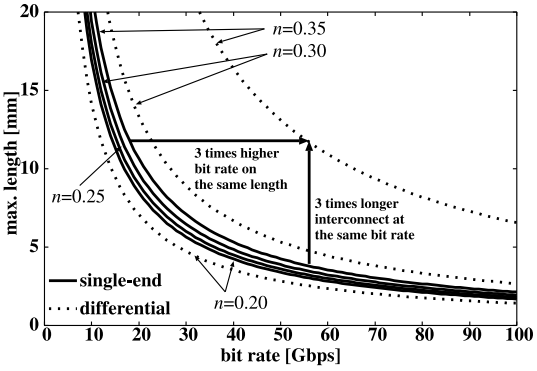

Fig. 10 Bit rate vs. maximum interconnect length with various attenuation. (high n means low attenuation.)

From the equations derived in Sect. 2, we can obtain the trade-off curve between bit rate and interconnect length. Figure 9 shows the curves of single-end signaling and differential signaling. The condition is the same as that of Sect. 3. In Fig. 9, V_{req} means the required eye opening V_{eye} for signal comparison. V_{req} depends on the sensitivity and noise margin of the receiver. The trade-off curve of single-end signaling does not change so drastically by V_{req}. On the other hand, the trade-off curve of differential signaling strongly depends on V_{req}. As V_{req} becomes lower, the advantage of differential signaling becomes larger. Generally speaking, the comparison ability of differential receiver is higher, and differential signaling does not suffer from the integrity of the reference voltage given to the receiver [6]. If V_{req} is $0.25V_{dd}$, differential signaling can achieve 100 Gbps communications on 10 mm length interconnect. On the other hand, single-end signaling can perform 25 Gbps signaling on 10 mm length interconnects, and if the bit rate is 100 Gbps, interconnect length has to be within 2.5 mm.

Figure 10 shows the trade-off curves between length and bit rate with various attenuation parameter n. V_{req} is equal to $0.25V_{dd}$. From Fig. 10, the performance of differential signaling depends on the attenuation, and it gets close to single-end signaling as the attenuation becomes large, because V_{max} decreases.

From the above discussion, differential signaling is much superior to single-end signaling when V_{req} is small and n is not too small. Exploiting the better comparison characteristics of the differential receiver, we can receive the benefit of differential signaling.

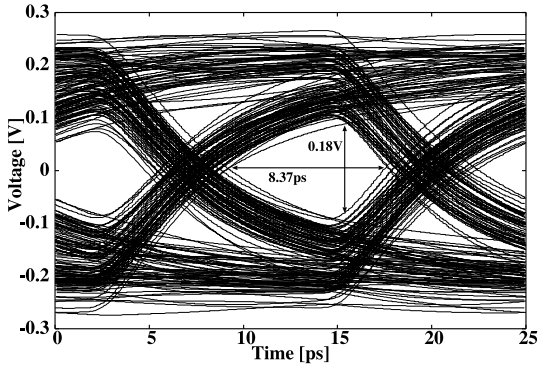

Fig. 11 Eye diagram of 80 Gbps signaling on 10 mm differential interconnect.

We show an example of eye diagram. Figure 11 is the eye diagram of 80 Gbps signaling on 10 mm differential transmission-line. From Fig. 11, the 80 Gbps signal transmission can be realized if the receiver sensitivity V_{req} is 0.15 V. The simulation conditions are the same as those explained in Sect. 3. The eye opening is roughly consistent with the analytical estimation and this result shows the validity of the analytical performance estimation.

5. Conclusion

The performance limitation of on-chip interconnect is discussed. It is important to know the maximum performance and performance trade-off to choose a proper signaling scheme. We first derive analytical expressions for performance estimation. By some assumptions, the maximum eye opening voltage is expressed by attenuation parameter n, interconnect length l and pulse shape. We then verify the analytical estimation by circuit simulation. The analytical estimation is valid in crosstalk-controlled interconnect structures even though the estimation does not consider crosstalk and dispersion. The analytical estimation gives trade-off curves of interconnect performance. In a practical situation in interconnect structure and receiver ability, differential signaling can perform 80 Gbps communication on 10 mm length interconnect. The simulation results suggest that a high bit rate can be achieved. However in such a condition, we have to consider more factors which degrade signal integrity such as waveform dispersion. The advantage of differential signaling is significant when the attenuation is not so severe.

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