Transistor Variability Modeling and its Validation With Ring-Oscillation Frequencies for Body-Biased Subthreshold Circuits

Hiroshi Fuketa, *Student Member, IEEE*, Masanori Hashimoto, *Member, IEEE*, Yukio Mitsuyama, *Member, IEEE*, and Takao Onoye, *Senior Member, IEEE*

***Abstract*—This paper presents transistor variability modeling and its validation for body-biased subthreshold circuits based on measurements of a device-array circuit using a 90-nm technology. The device array consists of p/nMOS transistors and ring oscillators. We examine and confirm the correlation between the performance variation model extracted from measured I-V characteristics and fabricated oscillation frequencies. We demonstrate that delay variations in subthreshold circuits are well characterized with two parameters, i.e., threshold voltage and subthreshold swing parameter. We also reveal that threshold voltage shift by body biasing can be deterministically modeled and statistical modeling is less meaningful.**

***Index Terms*—Body biasing, manufacturing variability, subthreshold circuit, threshold voltage, variability modeling.**

I. Introduction

VARIOUS subthreshold circuits have been proposed for ultra-low power applications [1]–[6]. Subthreshold circuits operate at a lower supply voltage than the threshold voltage ($V_{\rm th}$) of MOSFETs. Drain current in this region has an exponential dependence on $V_{\rm th}$, which means the circuit delay is extremely sensitive to manufacturing variability. However, the characterization of manufacturing variability focusing on subthreshold circuits has not been reported, whereas subthreshold leakage current has been measured [7], [8].

Circuits for measuring transistor variations have been proposed [7]–[12]. References [7] and [9] proposed device-array circuits and measured the variations in $V_{\rm th}$. Reference [10] described $V_{\rm th}$ isolation from measured data using an equation of MOSFET I-V characteristics. Reference [8] proposed a leakage-current sensor for measuring the subthreshold leakage current variations. In [11], variations in channel length and thickness of the gate oxide are extracted from the leakage currents of transistors and ring-oscillator (RO) frequencies. Reference [12] referred to measured $V_{\rm th}$ variations with ring oscillators. Although transistor-level variations such as $V_{\rm th}$ variation are well characterized in these papers, these papers focus on characterization for super-threshold circuits. As for variations in subthreshold circuits, the delay and energy variations are measured in [5], [6]. However, the correlation between performance variation of subthreshold circuits and transistor-level variations such as $V_{\rm th}$ variation was not discussed. When modeling the performance variation of subthreshold circuits, it is not clear whether more variation parameters need to be considered in addition to $V_{\rm th}$. In this study, we demonstrate transistor-level variation modeling of subthreshold characteristics and verify the correlation between the transistor-level modeling and the performance variations in subthreshold circuits. In addition, although the previous work [13] reported that simulations showing $V_{\rm th}$ variation is dominant in the subthreshold region, that work did not provide measurement verification. This work verifies that $V_{\rm th}$ variation is dominant in subthreshold circuits using measured RO frequencies.

Subthreshold circuits are sensitive to manufacturing variability, as previously mentioned. Therefore, post-silicon compensation techniques are crucial for subthreshold circuits to meet the required speed and power dissipation. Body biasing has been proposed as one possible technique [6], [14]. The variations of $V_{\rm th}$ with body-bias have been studied [15]–[17]. These papers explain that forward body-bias (FBB) reduces the standard deviation of $V_{\rm th}$ and reverse body-bias (RBB) increases that of $V_{\rm th}$ in comparison to zero body-bias (ZBB). However, it is not clear whether $V_{\rm th}$ shift due to body-bias can be deterministically modeled or should be statistically modeled, when transistors have large $V_{\rm th}$ variations.

We designed and fabricated a device-array circuit with variable body voltage, which alternately placed MOSFETs for measuring their I-V characteristics and ROs using a 90-nm technology. The preliminary work of this paper is presented in [18]. The contributions of this work are: 1) modeling within-die variations in subthreshold characteristics and validating them with RO frequencies; 2) modeling of $V_{\rm th}$ shift due to body-bias and validating it with RO frequencies. We reveal that subthreshold-current modeling with $V_{\rm th}$ and the subthreshold swing parameter can accurately reproduce variations in measured RO frequencies and also demonstrate that $V_{\rm th}$ shift due to body-bias depends on $V_{\rm th}$ but it can be deterministically modeled. This work is the first to explicitly verify the correlation between transistor-variability modeling and performance variations in subthreshold circuits taking body biasing into consideration.

The remainder of this paper is organized as follows. Section II describes the device-array circuit. Section III presents the mea-

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The authors are with the Department of Information Systems Engineering, Osaka University, Osaka 565-0871, Japan and also with JST, CREST, Tokyo 102-0075, Japan (e-mail: fuketa.hiroshi@ist.osaka-u.ac.jp; hasimoto@ist.osaka-u.ac.jp; mituyama@ist.osaka-u.ac.jp; onoye@ist.osaka-u.ac.jp).

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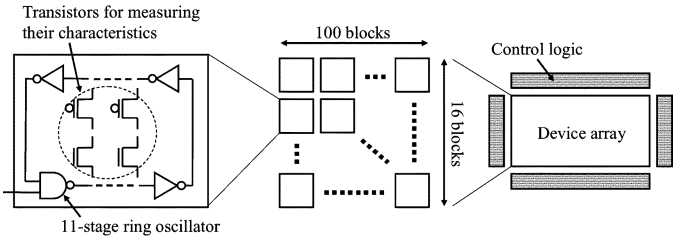


Fig. 1. Device-array structure.

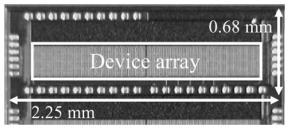


Fig. 2. Micrograph of test chip.

TABLE I
DEVICE COUNT IN DEVICE-ARRAY CIRCUIT

NMOS	3,200
PMOS	3,200
11-stage RO	1,600
23-stage RO	800
47-stage RO	400

sured results obtained for the device-array circuit and the characterization of variability. In Section IV, we discuss variations with body-bias. Finally, Section V concludes the paper.

II. DEVICE ARRAY CIRCUIT

A. Circuit Structure Overview

Fig. 1 outlines the device-array circuit designed to measure variations in MOSFET I-V characteristics and RO frequencies in the subthreshold region. The device array consists of 100×16 blocks. Each block contains two nMOSs and two pMOSs for measuring their I-V characteristics and an 11-stage RO. It is possible to evaluate the correlation between MOSFET I-V characteristics and RO frequencies by placing MOSFETs and ROs in the same area. The body voltage of MOSFETs and ROs can be changed. In addition, 23-stage and 47-stage ROs were integrated to reveal the relation between logic depth and variations in RO frequencies.

The test chip in Fig. 2 was fabricated in a 90-nm CMOS process with six metal layers and a triple-well structure, and the device-array circuit with a control logic and micro-pads occupies a 2.25 mm $\times$ 0.68 mm area. Table I lists the device count in the device-array circuit. The gate width of nMOSs is 0.54 μm and that of pMOSs is 0.82 μm, and these gate widths are used in the standard-sized ($1\times$) inverter. In addition, we implemented another device-array circuit on the same chip where the gate widths of both nMOS and pMOS are 0.15 μm, which is the minimum gate width in this process. In the rest of this paper, we have assumed the gate widths of transistors are 0.54 μm for nMOSs and 0.82 μm for pMOSs, unless otherwise stated.

B. Circuit for Measuring MOSFET Characteristics

Fig. 3 is a diagram of the circuit used to measure MOSFET I-V characteristics. We designed the circuit based on the transistor-array circuit proposed in [7] to accurately measure small subthreshold currents. We improved [7] such that both pMOS and nMOS characteristics could be measured. In addition, the body-bias of MOSFETs could be changed in the designed array. In Fig. 3, VPW is the body voltage of the nMOS and VNW is that of the pMOS.

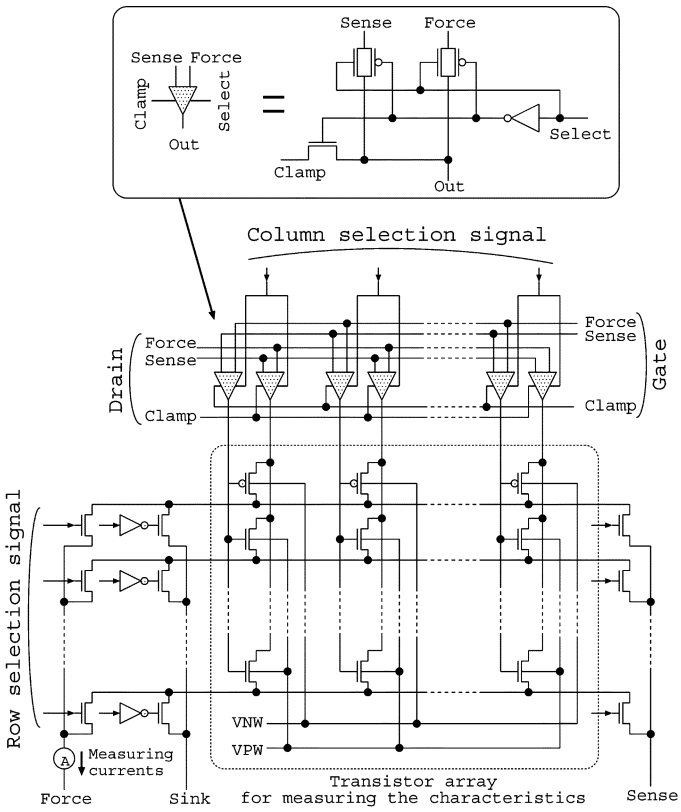


Fig. 3. Circuit for measuring MOSFET I-V characteristics.

The transistor for measuring MOSFET I-V characteristics was selected by using a column-selection signal and a row-selection signal. The force and sense pins of the drain, gate, and source can be used for Kelvin connection to eliminate the influence of parasitic wire resistance. Fig. 4 shows an example of connections when selecting a transistor in the dotted circle to be measured. The drains and gates of the transistors in the selected column are connected to the drain and gate force pins to which drain voltage and gate voltage are applied. The drains and gates of the transistors in the unselected columns are connected to the clamp pins. The sources of the transistors in the selected row are connected to the force pin to which source voltage is applied. The sources of the transistors in the unselected rows are connected to the sink pin. The sink pins are connected to GND. The sense pins of gate, drain and source are used to sense the voltages given to the transistor. In order to eliminate the leakage currents of the transistors in the unselected row, the voltage of the drain clamp pin is set to 0 V. In addition, the voltage of the gate clamp pin is adjusted to minimize the leakage currents of the unselected transistors. The I-V characteristics of the selected transistor can be measured by observing the current in the source force pin.

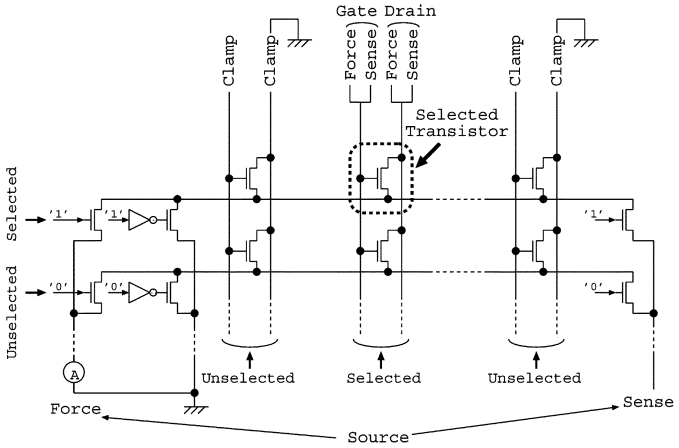


Fig. 4. Example of connections for measuring a transistor.

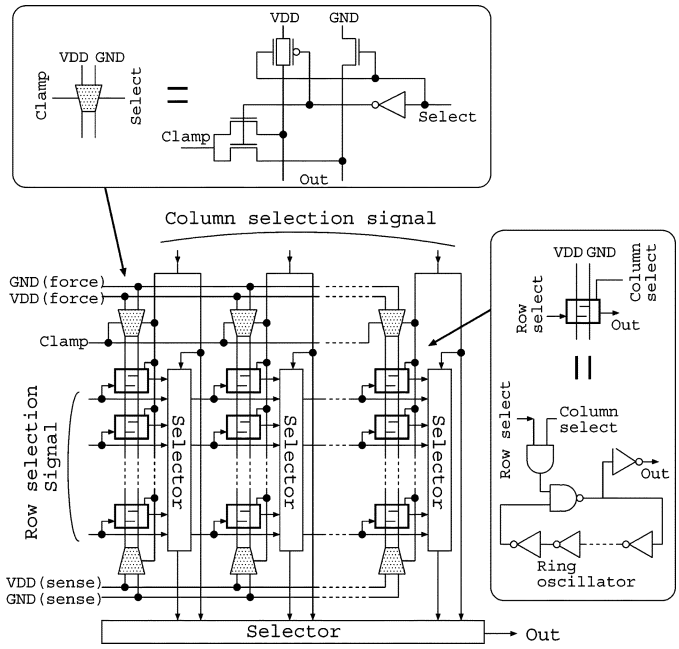


Fig. 5. Circuit for measuring RO frequencies.

C. Circuit for Measuring Ring Oscillator Frequencies

Fig. 5 shows the circuit for measuring RO frequencies. The VDD and GND of ROs in the unselected columns are connected to the clamp pin whose voltage is set to 0 V. The selector consists of tri-state buffers with a hierarchical structure (see Fig. 6) to ensure the operation in the subthreshold region [2]. Fig. 6 also illustrates an example of RO output selection. In subthreshold operation, leakage currents of unselected tri-state buffers are likely to be comparable to drive currents of selected buffers, which may disturb the selector operation. By limiting the number of tri-state buffers in parallel, we suppress the influence of the leakage currents and ensure the selector operation. The array circuit is designed such that the body-bias of ROs can be changed. The output of the ROs is divided by 1024 and measured.

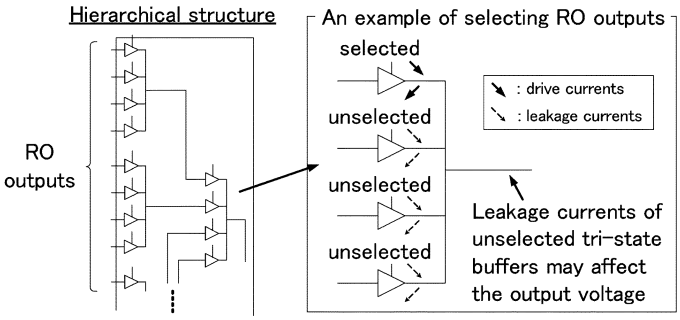


Fig. 6. Selector of RO outputs. The selector consists of tri-state buffers with a hierarchical structure.

TABLE II
RELATION BETWEEN NUMBER OF STAGES AND FREQUENCIES OF ROS IN A SINGLE CHIP ($V_{\rm DD} = 0.3$ V)

Number of stages	Frequencies (divided by 1,024)		
	μ [KHz]	σ [KHz]	σ/μ [%]
11	24.7 (24.61 – 24.79)	1.9 (1.84 – 1.97)	7.6
23	11.7 (11.66 – 11.74)	0.63 (0.600 – 0.662)	5.3
47	5.89 (5.868 – 5.912)	0.22 (0.206 – 0.236)	3.8

*Values in parentheses denote the 95% confidence interval.

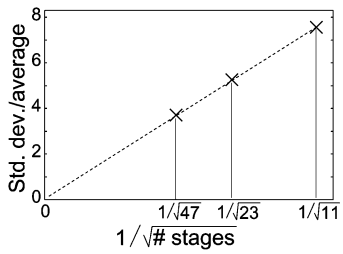


Fig. 7. Number of stages versus σ/μ of RO frequencies.

III. MEASURED RESULTS AND VARIABILITY CHARACTERIZATION

A. Variations in RO Frequencies

Table II lists the standard deviation/mean (σ/μ) of measured 11-stage, 23-stage, and 47-stage RO frequencies at $V_{\rm DD} = 0.3$ V in a chip. Fig. 7 shows that the σ/μ is nearly proportional to $1/\sqrt{N}$, where N is the number of RO stages. If the delay variations of each inverter in ROs are completely random and independent, σ/μ is proportional to $1/\sqrt{N}$. On the other hand, if the within-die delay variation has a correlation, for instance due to spatially correlated variation, σ/μ is not proportional to $1/\sqrt{N}$. In case that the correlation coefficient is 1, for example, σ/μ becomes independent of the number of RO stages. Fig. 7 implies that independent random variations are dominant in the within-die delay variations of subthreshold circuits and spatially correlated variations are not dominant in the area of the device array. Thus uncorrelated random variations in devices should be considered as a primary concern in designing subthreshold circuits.

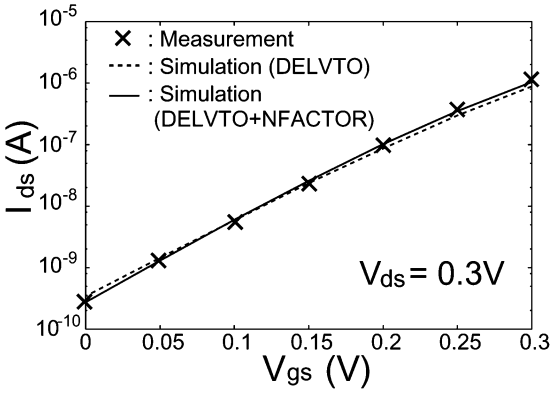


Fig. 8. Example of measured and simulated I-V characteristics.

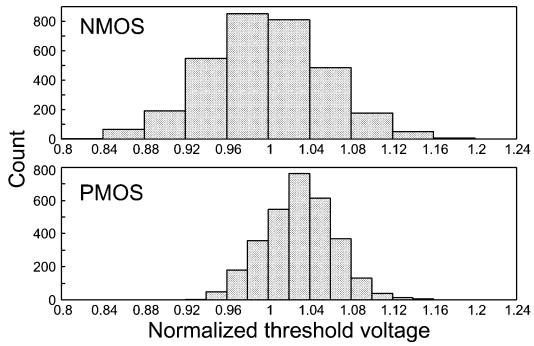


Fig. 9. Distribution of DELVTO parameters corresponding to $V_{\rm th}$ variations.

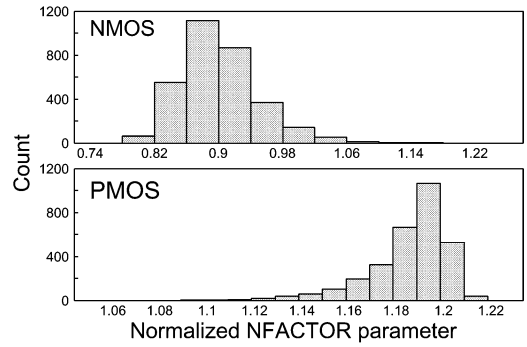


Fig. 10. Distribution of NFACTOR parameters corresponding to n variations.

B. Characterizing Variations

Here, we discuss how to model MOSFET variations from measured I-V characteristics. We focus on the modeling of within-die variations using measured characteristics in a single chip in this section. The drain current, I_{ds}, in the subthreshold region is expressed in the BSIM4 model [19] as

$$I_{ds} = I_0 e^{V_{gs} - V_{\rm th} - V_{\rm off}/nV_t} \left(1 - e^{-V_{ds}/V_t}\right) \tag{1}$$

where

$$I_0 = \mu \frac{W}{L} \sqrt{\frac{q\varepsilon_{\rm si}{\rm NDEP}}{2\Phi_s}} V_t^2. \tag{2}$$

Here, n is the subthreshold swing parameter, $V_{\rm off}$ is the offset voltage, and V_t is the thermal voltage. $V_{\rm off}$ is one of device parameters that aim to express I_{ds} when V_{gs} is 0 V. The $\varepsilon_{\rm si}$ is the dielectric constant of Si, NDEP is the doping concentration, and Φ_s is the surface potential. In (1), the $e^{V_{gs} - V_{\rm th} - V_{\rm off}/nV_t}$ term is dominant. Reference [7] reports that n as well as $V_{\rm th}$ vary. We thus considered the manufacturing variability of both $V_{\rm th}$ and n in this work to characterize variations accurately.

We derive $V_{\rm th}$ and n from the measured I-V characteristics such that the sum of relative errors at seven measurement points between the measured and simulated currents can be minimized by numerical fitting. A parameter of DELVTO is used to change $V_{\rm th}$. However, it is impossible to change n directly. We used a parameter of NFACTOR (the subthreshold swing factor) to represent n variations. Subthreshold swing parameter n is expressed in BSIM4 as

$$n = 1 + {\rm NFACTOR} \cdot \frac{C_{\rm dep}}{C_{\rm oxe}} + \frac{{\rm Cdsc\_Term} + {\rm CIT}}{C_{\rm oxe}}. \tag{3}$$

$C_{\rm oxe}$ is the gate-oxide capacitance, $C_{\rm dep}$ is the depletion-layer capacitance, ${\rm Cdsc\_Term}$ is the coupling capacitance, and CIT is the interface trap capacitance. NFACTOR was originally introduced as an empirical parameter to compensate for errors in calculating depletion-width capacitance [19].

Fig. 8 plots an example of measured and simulated I_{ds}-V_{gs} characteristics at $V_{ds} = 0.3$ V with the extracted DELVTO and NFACTOR parameters. For comparison, we extracted a DELVTO parameter solely assuming the NFACTOR parameter was constant. The simulation results corresponding to this single parameter modeling with DELVTO are also plotted in Fig. 8. In terms of ON current ($V_{ds} = V_{gs} = 0.3$ V), the error between the measurement and the simulation results of DELVTO modeling is 24%, whereas it reduces to 9% in the simulation with DELVTO and NFACTOR modeling.

Performing extraction for all transistors in a single chip, we can obtain the distributions for within-die DELVTO and NFACTOR variations that express $V_{\rm th}$ and n variations. Fig. 9 is a histogram of the distribution for DELVTO parameters corresponding to $V_{\rm th}$ variations in a single chip when $V_{ds} = 0.3$ V. Fig. 10 is a histogram of the distribution for NFACTOR parameters corresponding to n variations in a single chip when $V_{ds} = 0.3$ V. NFACTOR is normalized by the nominal value obtained from SPICE model card given from the foundry. Both nMOS $V_{\rm th}$ and pMOS $V_{\rm th}$ are normally distributed. The σ of nMOS $V_{\rm th}$ is larger than the σ of pMOS $V_{\rm th}$ because the channel width of nMOS is smaller than that of pMOS by 35%.

The exclusion of outliers is critically important in handling measurement data to create a reasonable statistical model, since some outliers lead the average and standard deviation to totally inappropriate values. We excluded these values using subthreshold swing parameter n in this paper. The n can be calculated from the measured data according to (1). We defined n as the slope between $V_{gs} = 0.05$ V and $V_{gs} = 0.15$ V at $V_{ds} = 0.3$ V for an nMOS, and $V_{gs} - 0.15$ V and $V_{gs} = -0.05$ V at $V_{ds} = -0.3$ V for a pMOS. Fig. 11 is a histogram of the distribution for n calculated from the measured data. In 96% of pMOSs, n is no more than 1.6 and the rest is widely distributed. For example, Fig. 12(a) plots the measured and simulated results with DELVTO and NFACTOR modeling for a pMOS with $n = 1.55$. The normalized NFACTOR is 1.14, and the average error between them is 7.4%. Fig. 12(b) plots the measured and

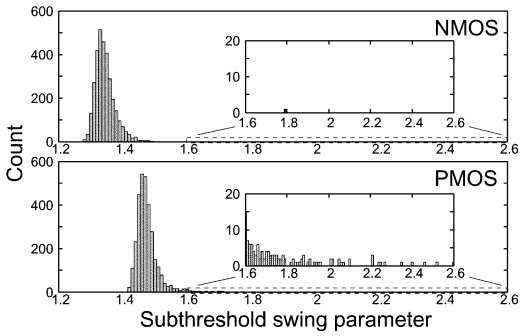


Fig. 11. Subthreshold swing parameter n calculated from measured data.

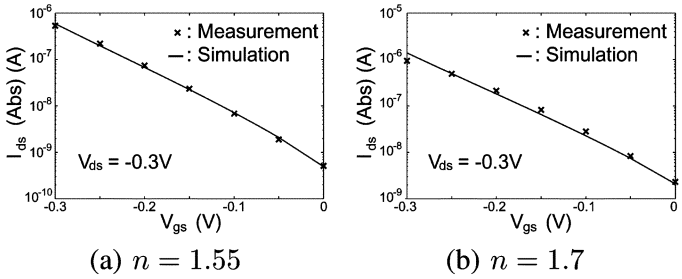


Fig. 12. Measured and simulated I-V characteristics of pMOS.

simulated results for a pMOS with $n = 1.7$, where the lower bound of the normalized NFACTOR is in parameter fitting set to 1.1 which is equivalent to $n = 1.6$. In this case, the average error is 18%, and the current is not modeled accurately. Without the lower bound of the normalized NFACTOR, the average error could be reduced, but the normalized NFACTOR jumps to 0.94, which is much farther from the distribution in Fig. 10. This means it is difficult to reproduce the I-V characteristics of large n transistors by adjusting DELVTO and NFACTOR in the given BSIM4 model. We thus excluded these transistors for the parameter extraction process since extracted parameters from these transistors could lead the average and standard deviation of parameter variations to totally inappropriate values. In this study, we decided to exclude to exclude transistors of $n > 1.6$. One nMOS (0.03%) and 125 pMOSs (4%) in the device array were excluded. The 95% confidence interval of μ of normalized $V_{\rm th}$ is 0.999 to 1.001 for pMOS and 0.998 to 1.002 for nMOS, and that of σ of normalized $V_{\rm th}$ is 0.976 to 1.025 for both pMOS and nMOS.

Finally, let us discuss the correlation coefficients between the two parameters. The correlation coefficient between DELVTO and NFACTOR of nMOS is 0.042 and that of pMOS is 0.069. The correlation coefficient between nMOS and pMOS of DELVTO is 0.016 and that of NFACTOR is 0.0025. As all the correlation coefficients are below 0.1, we consider the distributions to have almost no correlation.

We also extracted DELVTO and NFACTOR parameters for nMOS with $W = 0.15$ μm. Fig. 13 shows the distributions of those parameter variations. The standard deviation of $V_{\rm th}$ variation for NMOS with $W = 0.15$ μm is larger than that with $W = 0.54$ μm by 28%.

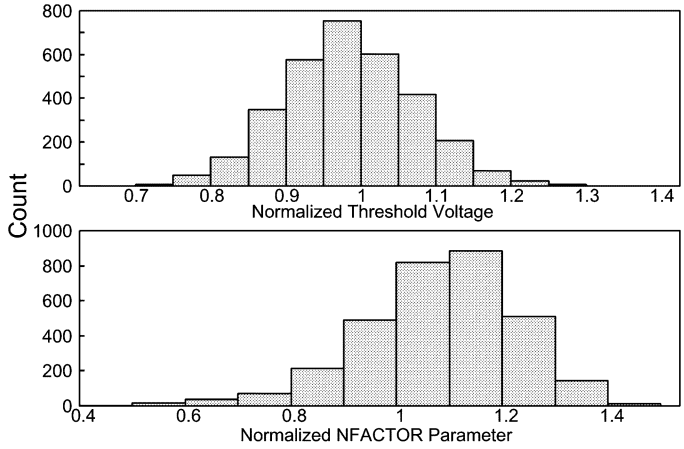


Fig. 13. Distribution of DELVTO and NFACTOR parameters of nMOS with $W = 0.15$ μm.

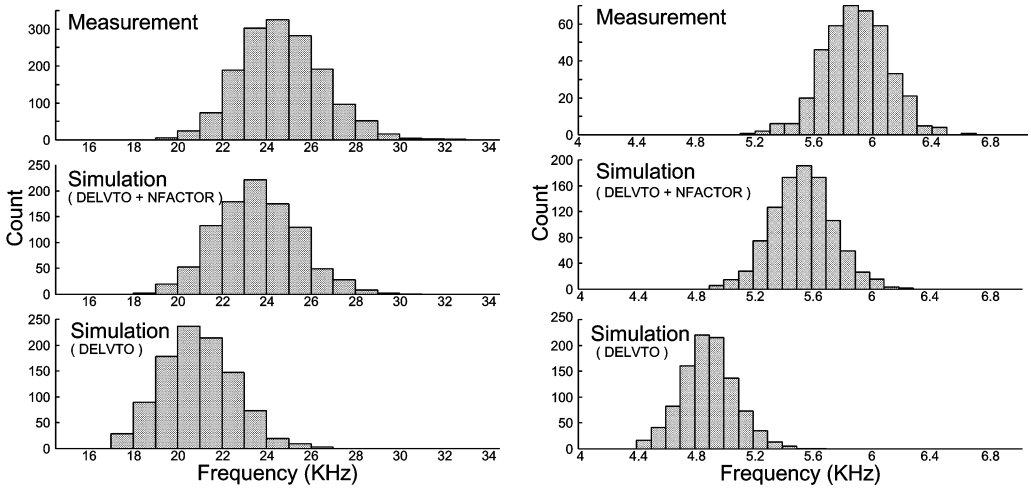
C. Evaluation of Variation Model

To validate the within-die variation model whose construction we discussed in Section III-B, we carried out circuit simulations and obtained RO frequencies with the variation model, and then compared the simulation results to those we measured in a certain chip.

Fig. 14 is a histogram of the distributions for 11-stage RO frequencies [see Fig. 14(a)] and 47-stage RO frequencies [see Fig. 14(b)] which were obtained by Monte Carlo simulations (1000 runs) with DELVTO and NFACTOR modeling, and with DELVTO modeling. We assumed that DELVTO and NFACTOR were normally distributed with no correlation. The distribution of NFACTOR will be discussed later. The parasitic capacitance and resistance were extracted by Star-RCXT. Table III lists the average (μ) and standard deviation (σ) of RO frequencies. There are significant differences in μ between the two models, and the distribution simulated with DELVTO and NFACTOR modeling was much closer to the measurements in both 11-stage and 47-stage ROs. The average frequency was underestimated by 16% when modeling variation with DELVTO only, whereas it was more accurately estimated within 6% error when both variations of DELVTO and NFACTOR were modeled. This means that variations in subthreshold circuits can be accurately analyzed with variation models of $V_{\rm th}$ and subthreshold swing parameter n.

We investigate the modeling at different supply voltages. In subthreshold circuits, 0.3–0.4 V is often used for the supply voltage [1], [2], [5], [6]. This is because leakage energy tends to be dominant below 0.3 V and the energy consumption does not necessarily decrease even if the supply voltage is lowered. Thus we validate the modeling at 0.25 and 0.35 V in addition to 0.3 V. Table IV lists μ and σ of 11-stage RO frequencies at $V_{\rm DD} = 0.25$ and 0.35 V. There are also significant differences between the two models, and the distributions simulated with DELVTO and NFACTOR modeling were much closer to the measurements as is the case at $V_{\rm DD} = 0.3$ V.

The above discussion assumes that NFACTOR is normally distributed. Strictly speaking, however, this assumption might be inappropriate. We thus investigated how the distribution of NFACTOR affected the estimation accuracy of RO-frequency



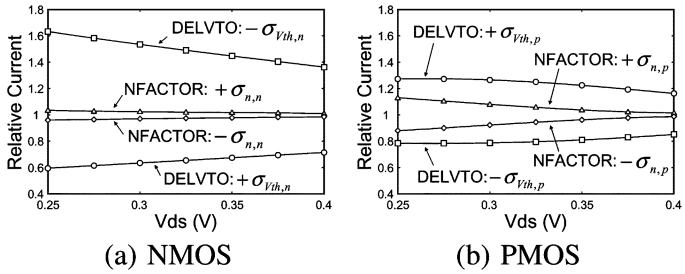
(a) 11-stage RO (b) 47-stage RO

Fig. 14. Measurements and simulations of RO frequencies ($V_{\rm DD} = 0.3$ V).

TABLE III
AVERAGE AND STANDARD DEVIATION OF RO FREQUENCIES ($V_{\rm DD} = 0.3$ V)

		Frequencies (divided by 1,024)		
		μ (KHz)	σ (KHz)	σ/μ (%)
11-stage RO	Measurement	24.7 (24.61 – 24.79)	1.9 (1.84 – 1.97)	7.6
	Simulation (DELVTO+NFACTOR)	23.6 (23.49 – 23.71)	1.8 (1.72 – 1.88)	7.7
	Simulation (DELVTO)	20.9 (20.80 – 21.00)	1.6 (1.53 – 1.67)	7.9
47-stage RO	Measurement	5.89 (5.868 – 5.912)	0.22 (0.206 – 0.236)	3.8
	Simulation (DELVTO+NFACTOR)	5.54 (5.527 – 5.553)	0.21 (0.201 – 0.220)	3.8
	Simulation (DELVTO)	4.89 (4.879 – 4.901)	0.18 (0.172 – 0.188)	3.8

*Values in parentheses denote the 95% confidence interval.



(a) NMOS (b) PMOS

Fig. 15. Influences of DELVTO and NFACTOR variations on ON currents in simulation. Relative current represents ON current with variations normalized by ON current with no variations at each V_{ds}. σ_{Vth} and σ_n represent standard deviations of within-die $V_{\rm th}$ and n variations, respectively.

TABLE IV
AVERAGE AND STANDARD DEVIATION OF 11-STAGE RO FREQUENCIES AT DIFFERENT SUPPLY VOLTAGES

V_{DD} (V)		Frequencies (divided by 1,024)		
		μ (KHz)	σ (KHz)	σ/μ (%)
0.25	Measurement	10.5 (10.45 – 10.55)	0.95 (0.918 – 0.984)	9.1
	Simulation (DELVTO+NFACTOR)	9.64 (9.584 – 9.696)	0.90 (0.862 – 0.941)	9.4
	Simulation (DELVTO)	8.55 (8.503 – 8.597)	0.76 (8.503 – 8.597)	8.8
0.35	Measurement	63.2 (63.02 – 63.38)	3.7 (3.58 – 3.83)	5.8
	Simulation (DELVTO+NFACTOR)	62.4 (62.15 – 62.65)	4.1 (3.93 – 4.29)	6.5
	Simulation (DELVTO)	48.3 (48.09 – 48.51)	3.4 (3.26 – 3.56)	7.1

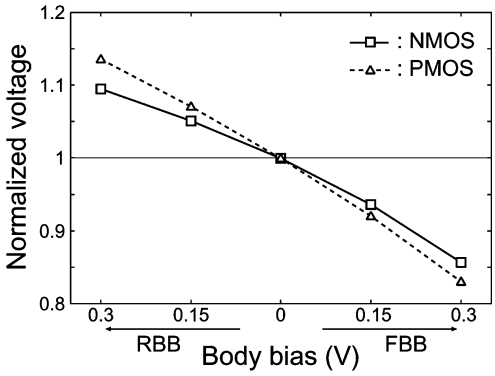
*Values in parentheses denote the 95% confidence interval.

TABLE V
INFLUENCES OF NFACTOR VARIATIONS ON ESTIMATION ACCURACY OF FREQUENCY VARIATION OF 11-STAGE RO

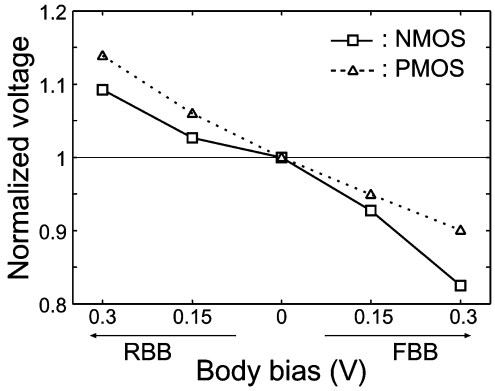
V_{DD} (V)		Frequencies (divided by 1,024)		
		μ (KHz)	σ (KHz)	σ/μ (%)
0.3	Measurement	24.7 (24.61 – 24.79)	1.9 (1.84 – 1.97)	7.6
	Simulation (w/ NFACTOR variations)	23.6 (23.49 – 23.71)	1.8 (1.72 – 1.88)	7.7
	Simulation (w/o NFACTOR variations)	23.7 (23.59 – 23.81)	1.8 (1.72 – 1.88)	7.6
0.25	Measurement	10.5 (10.45 – 10.55)	0.95 (0.918 – 0.984)	9.1
	Simulation (w/ NFACTOR variations)	9.64 (9.584 – 9.696)	0.90 (0.862 – 0.941)	9.4
	Simulation (w/o NFACTOR variations)	9.71 (9.654 – 9.766)	0.90 (0.862 – 0.941)	9.3
0.35	Measurement	63.2 (63.02 – 63.38)	3.7 (3.58 – 3.83)	5.8
	Simulation (w/ NFACTOR variations)	62.4 (62.15 – 62.65)	4.1 (3.93 – 4.29)	6.5
	Simulation (w/o NFACTOR variations)	62.7 (62.45 – 62.95)	4.1 (3.93 – 4.29)	6.6

*Values in parentheses denote the 95% confidence interval.

variations. Table V lists the influences of NFACTOR variations. Simulation without NFACTOR variations was conducted such that the standard deviation of NFACTOR was set to zero. There are no significant differences in μ and σ between simulation with and without NFACTOR variations. This means NFACTOR variations had a less influence on the estimation accuracy of delay variations. In order to discuss the reason, we examine the influences of DELVTO and NFACTOR variations on the ON currents ($V_{gs} = V_{ds}$) with simulation. We show the results in Fig. 15. In this figure, $\sigma_{Vth,n}$ and $\sigma_{Vth,p}$ denote standard deviations of within-die $V_{\rm th}$ variations for nMOS and for pMOS respectively, and $\sigma_{n,n}$ and $\sigma_{n,p}$ represent standard deviations of within-die n variations for nMOS and for pMOS, respectively. Relative current represents ON current with variations ($\pm\sigma_{Vth}$ or $\pm\sigma_n$) normalized by ON current with no variations at each V_{ds}. For example, "DELVTO: $+\sigma_{Vth,n}$" means normalized ON current of a nMOS whose $V_{\rm th}$ is shifted by $+\sigma_{Vth,n}$ and n remains a nominal value. This figure indicates that the impact of



(a) Average (μ)



(b) Standard deviation (σ)

Fig. 16. Average and standard deviation of $V_{\rm th}$ shift due to body-bias.

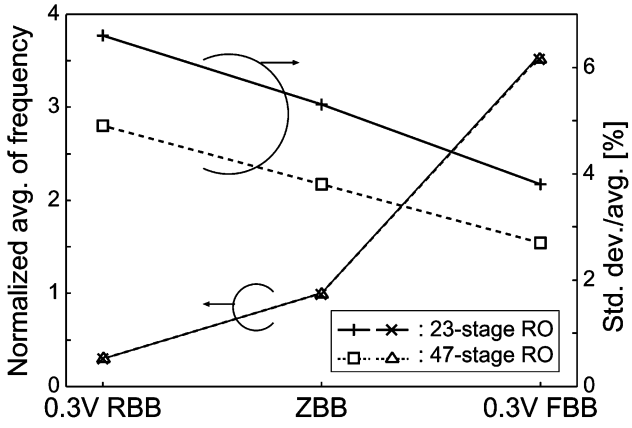


Fig. 17. μ and σ/μ of RO frequencies with body-bias.

TABLE VI
AVERAGE AND STANDARD DEVIATION OF RO FREQUENCIES WITH BODY-BIAS ($V_{\rm DD}$ = 0.3 V)

		Frequencies (divided by 1,024)		
		μ [KHz]	σ [KHz]	σ/μ [%]
23-stage RO	FBB (0.3 V)	41.8	1.6	3.8
	ZBB	11.7	0.63	5.3
	RBB (0.3 V)	3.49	0.23	6.6
47-stage RO	FBB (0.3 V)	21.0	0.55	2.7
	ZBB	5.89	0.22	3.8
	RBB (0.3 V)	1.76	0.23	4.9

DELVTO ($V_{\rm th}$) fluctuation on ON current is larger than that of NFACTOR (n) fluctuation. This is the reason why NFACTOR variations had a less influence on the estimation accuracy of delay variations as shown in Table V. Fig. 15 shows a tendency that the impact of NFACTOR increases as the supply voltage decreases, however even at $V_{\rm DD}$ = 0.25 V, the influence of NFACTOR variation on RO frequency is negligible as explained in Table V.

We thus conclude that the consideration of n variation (NFACTOR) in addition to $V_{\rm th}$ variation (DELVTO) is important for modeling subthreshold I-V characteristics, in other words, for obtaining appropriate $V_{\rm th}$. However, NFACTOR variation itself is a secondary effect on estimating delay variation when $V_{\rm DD}$ is in the range between 0.25 and 0.35 V, which is a practical voltage range for subthreshold circuits from the point of view of energy efficiency [1].

IV. EVALUATION OF BODY-BIAS EFFECT

This section discusses the body-bias effect based on the measured results of I-V characteristics and RO frequencies. We explain the modeling of the body-bias effect and our evaluation of the model.

A. Measured Results

We measured the $I_{ds} - V_{gs}$ characteristics at V_{ds} = 0.3 V with various body-bias voltages. DELVTO and NFACTOR were extracted from the measured results similarly to the way they were described in Section III. Fig. 16(a) plots the average (μ) of $V_{\rm th}$ and Fig. 16(b) plots the deviation (σ) of $V_{\rm th}$ with various body-bias voltages in a single chip. The μ and σ are normalized by those at ZBB. The 0.3-V forward body-bias (FBB) decreases the average of V_{th} by 15% for nMOSs and 17% for pMOSs. The 0.3-V reverse body-bias (RBB) increases the average of V_{th} by 9% for nMOSs and 14% for pMOSs. In addition, the standard deviation of $V_{\rm th}$ is decreased by FBB and is increased by RBB. This result is consistent with the analysis of super-threshold circuits in previous works [15], [16].

We also measured the RO frequencies at $V_{\rm DD}$ = 0.3 V with 0.3-V FBB and 0.3-V RBB in a single chip. Table VI and Fig. 17 show the μ and σ of 23-stage and 47-stage RO frequencies with ZBB, 0.3-V FBB, and 0.3-V RBB. The μ of both 23-stage and 47-stage RO frequencies at 0.3-V FBB is 3.6 $\times$ higher than that at ZBB, and σ/μ improves by around 1%. However, the μ of both 23-stage and 47-stage RO frequencies at 0.3-V RBB is smaller than that at ZBB by 70%, and σ/μ deteriorates by 1%. FBB reduces not only circuit delays but also their variations, whereas RBB increases circuit delays and their variations.

B. Modeling of Body-Bias Effect

For long-channel MOSFETs, $V_{\rm th}$ can be expressed [20] as

$$V_{\rm th} = V_{\rm FB} + 2\psi_B + \gamma\sqrt{2\psi_B - V_{bs}} \tag{4}$$

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_{\rm si}}}{C_{\rm ox}} \tag{5}$$

where $V_{\rm FB}$ is the flat-band voltage, ψ_B is the Fermi level from the intrinsic Fermi level, and N_A is the impurity concentration. Here, V_{bs} is the body-source voltage and $C_{\rm ox}$ is the gate oxide capacitance per area. The impurity concentration N_A is fluctuated by random dopant fluctuations (RDFs), which leads to $V_{\rm th}$

variation. Reference [21] reports that the fluctuations of $V_{\rm th}$ are mainly caused by RDFs. Thus the fluctuation of γ, which is a function of N_A, should be considered for $V_{\rm th}$ variations. In the following discussion, we treat γ as a variable corresponding to $V_{\rm th}$.

In short-channel MOSFETs, $V_{\rm th}$ is affected by various effects such as drain induced barrier lowering (DIBL), the short channel effect, and the narrow width effect. To take these effects into account, we introduced $V_{\rm base}$, which includes voltage shift due to these effects in addition to $V_{\rm FB}+2\psi_B$. Using $V_{\rm base}$, we write $V_{\rm th}$ for short-channel MOSFETs as

$$V_{\rm th}(\gamma, V_{bs}) = V_{\rm base} + \gamma\sqrt{2\psi_B - V_{bs}}. \tag{6}$$

We defined α as the body-bias effect that represents the voltage shift from $V_{\rm th}$ at ZBB due to body-bias. The dependence of $V_{\rm th}$ on body-bias is mostly included in $\gamma\sqrt{2\psi_B - V_{bs}}$; $V_{\rm base}$ is less sensitive to body-bias compared to $\gamma\sqrt{2\psi_B - V_{bs}}$. We thus derive a simplified model of body-bias effect $\alpha(\gamma, V_{bs})$ for nMOS assuming the dependence of $V_{\rm base}$ on V_{bs} is negligibly small

$$\alpha(\gamma, V_{bs}) = \frac{V_{\rm th}(\gamma, V_{bs})}{V_{\rm th}(\gamma, 0)} = \frac{V_{\rm base} + \gamma\sqrt{2\psi_B - V_{bs}}}{V_{\rm base} + \gamma\sqrt{2\psi_B}}. \tag{7}$$

The nominal values in this process of $V_{\rm th}$, γ, and ψ_B can be obtained from the SPICE model card. $V_{\rm base}$ is calculated from the nominal $V_{\rm th}$, γ, and ψ_B in (6) when $V_{bs} = 0$ V. Below, we validate the simplified analytical model of body-bias effect α of (7).

Fig. 18 shows a simplified analytical model of body-bias effect $\alpha(\gamma, V_{bs})$ in (7). The lines in the figure are plotted as a function of γ at each body-bias voltage, and γ is converted to $V_{\rm th}$ using (6). The horizontal axis represents $V_{\rm th}$ at ZBB ($V_{\rm th}(\gamma, 0)$) and is normalized by the nominal $V_{\rm th}$ of the SPICE model card. The 0.3-V FBB means $V_{bs} = 0.3$ V and 0.3-V RBB means $V_{bs} = -0.3$ V for an nMOS. The α of both nMOS and pMOS looks almost constant, but it has a gentle slope. When $V_{\rm th}$ fluctuates from the -20% of the nominal $V_{\rm th}$ to +20%, α at 0.3-V FBB varies from 0.849 to 0.864 for an nMOS. In comparison to the case when α is considered to be 0.855 (@ nominal $V_{\rm th}$) as a constant, the maximum difference is 0.009, which is equivalent to 4 mV and is around 1% of $V_{\rm th}$. The difference for a pMOS is smaller than that for an nMOS. The error caused by regarding α as a constant is smaller than the $V_{\rm th}$ variation and its impact is limited.

Fig. 19 shows the measured body-bias effect with various body-bias voltages in a single chip. Each dot corresponds to the body-bias effect calculated from the measured $V_{\rm th}$ of each transistor in the device array. The measured results indicate that the body-bias effect α is almost constant. Fig. 20 compares the measured results to the simplified analytical model of the body-bias effect in (7) when γ is a nominal value. The measured results represent the average values of the body-bias effect calculated from the measured $V_{\rm th}$ of every transistor. The measured body-bias effect is consistent with the simplified analytical model (7).

Strictly speaking, the measured body-bias effect fluctuates slightly as can be seen in Fig. 19, and the standard

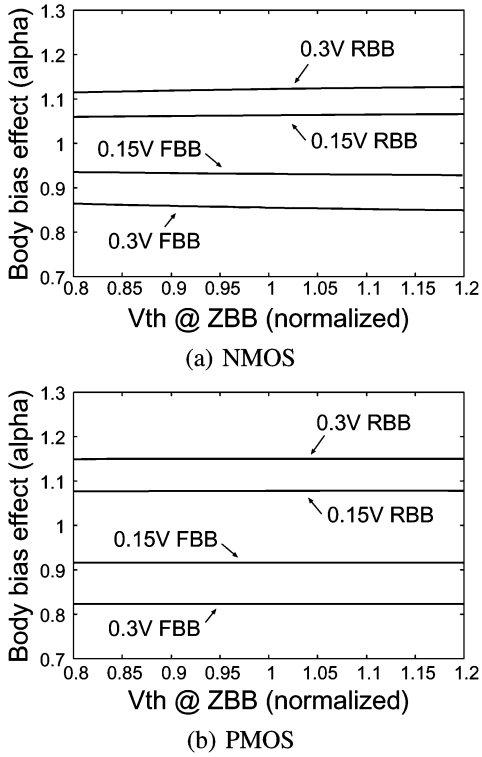


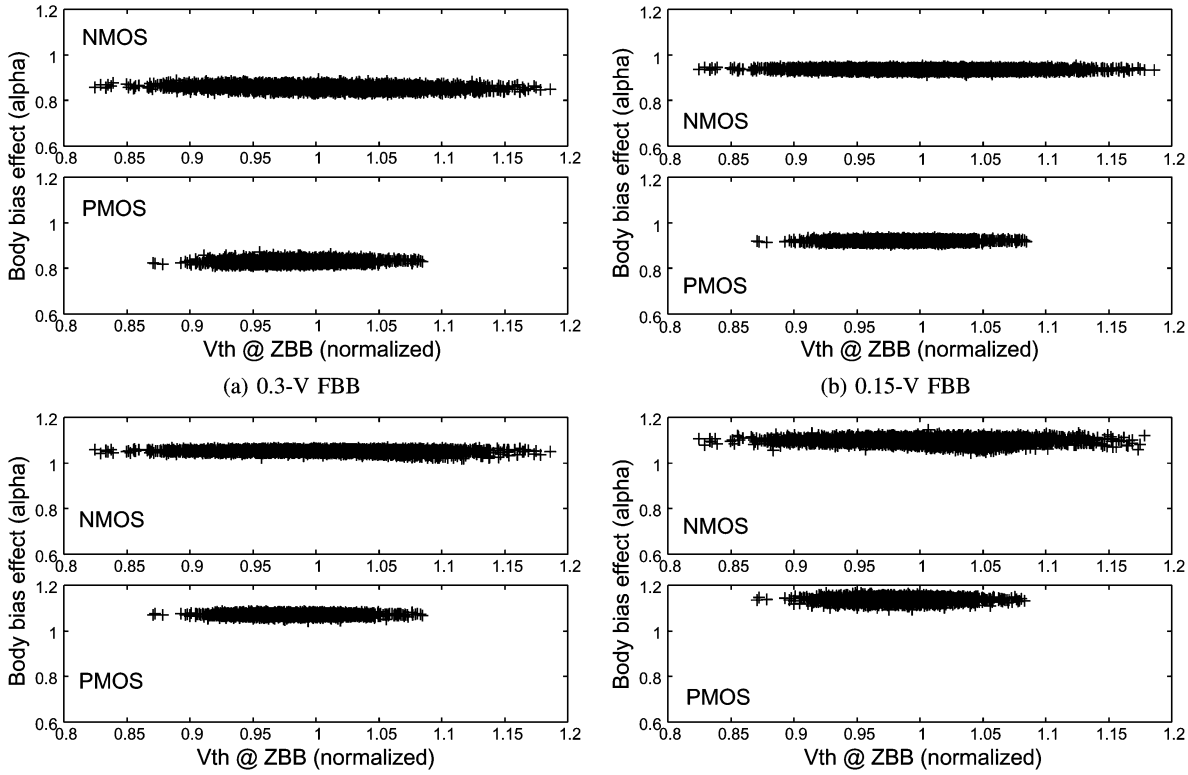
Fig. 18. Simplified analytical model of body-bias effect in (7) as a function of $V_{\rm th}$ at ZBB.

deviations are up to 0.012. In order to investigate how this fluctuation impacts on circuit delay estimation, we examine ON ($|V_{gs}| = |V_{ds}| = V_{\rm DD}$) currents. A standard deviation of the measured body-bias effect fluctuation corresponds to $-9\%-+9\%$ (nMOS) and $-7\%-+7\%$ (pMOS) ON current variation, whereas $-37\%-+54\%$ (nMOS) and $-21\%-+27\%$ (pMOS) in the case of $V_{\rm th}$ variation. Therefore, the influence of the $V_{\rm th}$ fluctuation on circuit delay estimation dominates that of the measure body-bias effect variation due to squared-root operation in calculation of standard deviation, and the fluctuation of the measured body-bias effect can be ignored.

Figs. 19 and 20 indicate that body-bias effect α can be considered as a constant and it can be modeled deterministically but not statistically. We will discuss our validation of this deterministic modeling with RO frequencies in Section IV-C.

1) Dependence on Die-to-Die $V_{\rm th}$ Variations: Body-bias effect α has no dependences on $V_{\rm th}$ at ZBB. This means body-bias effect α is independent of not only within-die $V_{\rm th}$ variations but also die-to-die $V_{\rm th}$ variations. Table VII lists measured body-bias effect α at 0.3-V FBB in four chips. The values in the "measurement" column represent the average value of measured body-bias effects of the each chip, and the values in the "model" column are calculated using the simplified analytical model (7) with the nominal values in the SPICE model card given from the foundry.

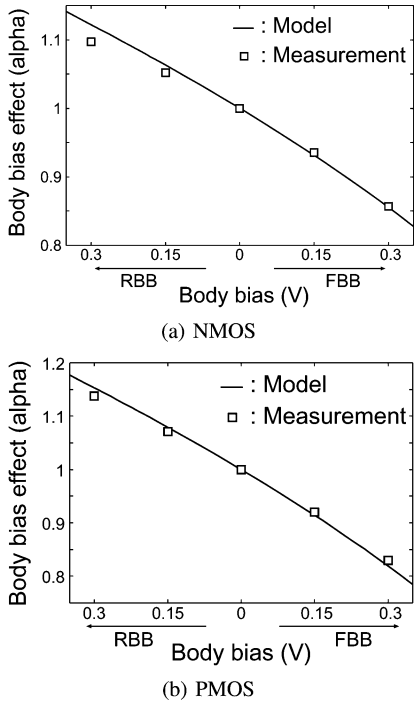
The standard deviations of measured body-bias effects for the four chips are 0.007 (0.8% of the average) for pMOS and 0.001 (0.1%) for nMOS. In addition, the averages of relative errors between the measured body-bias effects and the simplified analytical model are 0.9% for pMOS and 0.2% for nMOS. The differ-



(a) 0.3-V FBB (b) 0.15-V FBB

(c) 0.15-V RBB (d) 0.3-V RBB

Fig. 19. Measured body-bias effect α, which is defined as $V_{\rm th}$ with body-bias divided by $V_{\rm th}$ at ZBB. Each dot corresponds to each transistor.



(a) NMOS

(b) PMOS

Fig. 20. Comparison of measured results (average values of body-bias effects obtained from measured $V_{\rm th}$ of every transistor) to simplified analytical model of body-bias effect in (7).

ences among the chips are so small that we conclude body-bias effect is also constant regardless of the chip and close to the model value.

TABLE VII
BODY-BIAS EFFECT AT 0.3-V FBB IN VARIOUS CHIPS

	Measurement				Model
	Chip #1	Chip #2	Chip #3	Chip #4	
PMOS	0.81	0.83	0.83	0.83	0.819
NMOS	0.85	0.86	0.86	0.86	0.854

2) Dependence on Temperature: Body-bias effect α depends on temperature T. The dependence for an nMOS can be derived as

$$\frac{d\alpha}{dT} = \frac{A}{\left(V_{\rm base} + \gamma\sqrt{2\psi_B}\right)^2} \tag{8}$$

$$\begin{aligned} A =& \gamma\left(\sqrt{2\psi_B} - \sqrt{2\psi_B - V_{bs}}\right)\frac{dV_{\rm base}}{dT} \\ &+ \gamma V_{\rm base}\left(\frac{1}{\sqrt{2\psi_B - V_{bs}}} - \frac{1}{\sqrt{2\psi_B}}\right)\frac{d\psi_B}{dT} \\ &+ \gamma^2\left(\frac{V_{bs}}{\sqrt{2\psi_B(2\psi_B - V_{bs})}}\right)\frac{d\psi_B}{dT}. \end{aligned} \tag{9}$$

In the case of an nMOS ($W = 0.54\ \mu$m), $d\alpha/dT$ is less than zero when FBB ($V_{bs} > 0$), and $d\alpha/dT$ is more than zero when RBB ($V_{bs} < 0$) because conditions $V_{\rm base} > 0$, $dV_{\rm base}/dT < 0$, and $d\psi_B/dT < 0$ are met when the temperature is between 20 °C and 100 °C. This means that the body-bias effect increases due to the rise in temperature. Fig. 21 plots the average measured body-bias effect in a single chip and the simplified analytical model of the body-bias effect in (7) as a function of temperature. We can see that the measured results are consistent with the dependence on temperature, which is indicated by

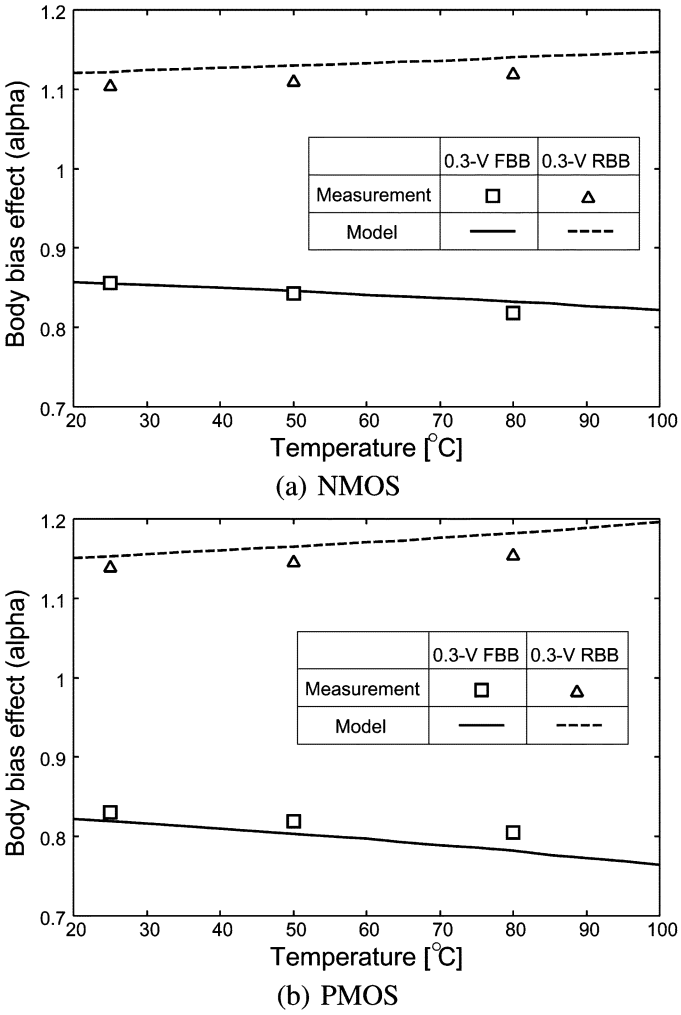


Fig. 21. Measured body-bias effect and simplified analytical model of the body-bias effect in (7) as a function of temperature. Measured results are average values of body-bias effects obtained from measured $V_{\rm th}$ at each temperature.

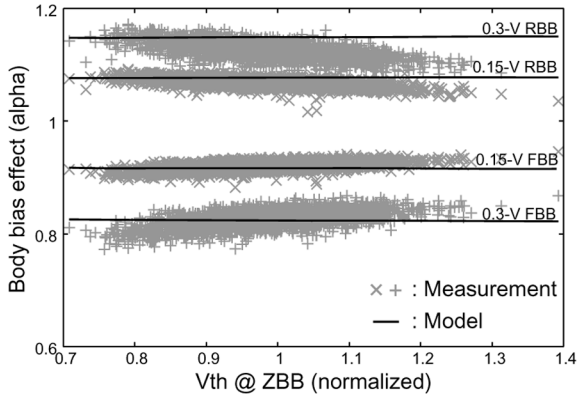


Fig. 22. Body-bias effect (α) of nMOS with narrow gate width ($W = 0.15\ \mu$m). Each dot corresponds to measured body-bias effect at each transistor. Each line represents simplified analytical model in (7).

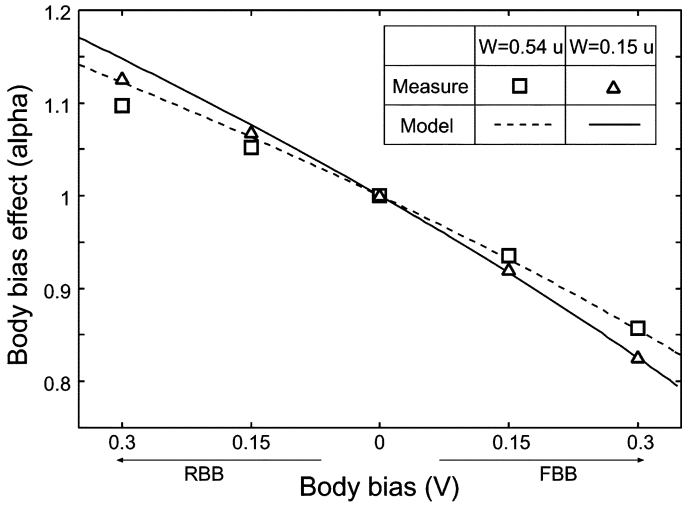


Fig. 23. Body-bias effect (α) of nMOS with different widths. Measured body-bias effects are average values of body-bias effects obtained from measured $V_{\rm th}$.

the simplified analytical model, whereas there are slight errors between measured results and model values. This is because the simplified analytical model is calculated with the nominal values obtained from the SPICE model card of this process and these nominal values do not perfectly fit to the measured chip.

3) Dependence on Transistor Size: The body-bias effect also depends on transistor size since $V_{\rm base}$ depends on the gate width in (7). Fig. 22 shows the body-bias effect of an nMOS with a narrow gate width ($W = 0.15\ \mu$m). Each dot corresponds to measured body-bias effect at each transistor in a single chip. The lines in Fig. 22 represent the simplified analytical model of the body-bias effect in (7). Fig. 23 plots the measured body-bias effects, which represent the average values of body-bias effects obtained from the measured $V_{\rm th}$ of all transistors in a single chip, and the simplified analytical model (7) in a $W = 0.15\ \mu$m nMOS. The results for a $W = 0.54\ \mu$m nMOS are also plotted, which are the same as those in Fig. 20(a). The measured body-bias effect of $W = 0.15\ \mu$m in FBB is smaller than that of $W = 0.54\ \mu$m, which is consistent with the simplified analytical model. Also in the case of RBB, the measured body-bias effect and the simplified analytical model are consistent. Fig. 23 shows the body-bias effect for $W = 0.15\ \mu$m nMOSs is steeper than that for $W = 0.54\ \mu$m nMOSs. This indicates that the body-bias effect for a $W = 0.54\ \mu$m nMOS is closer to 1 than that for a $W = 0.15\ \mu$m nMOS. Body-bias effect α which is closer to 1 means that V_{th} shift due to body-bias is smaller, therefore, $V_{\rm th}$ shift for a $W = 0.15\ \mu$m nMOS is larger than that for a $W = 0.54\ \mu$m nMOS. This means that $V_{\rm th}$ for a nMOS with $W = 0.15\ \mu$m is more controllable.

C. Verification of Body-Bias Effect Model

To verify the deterministic body-bias effect model discussed in the previous section, we compared RO frequencies simulated with the model and the measurement results. In the simulation, DELVTO was shifted with constant ratio α due to body-bias and given to the simulator. For the simulation at 0.3-V FBB, we use $\alpha = 0.86$ for the nMOS and $\alpha = 0.82$ for the pMOS. For instance, a nMOS with DELVTO = 10 mV at ZBB is modified to nMOS with DELVTO = 8.6 mV at 0.3-V FBB. For NFACTOR, the offset caused by body biasing, which is the average difference between NFACTORs at ZBB and FBB, is added to the

TABLE VIII
MEASURED AND SIMULATED 23-STAGE RO FREQUENCIES AT 0.3-V FBB ($V_{\rm DD} = 0.3$ V)

	Frequencies (divided by 1,024)		
	μ [KHz]	σ [KHz]	σ/μ [%]
Measurement	41.8 (41.69 – 41.91)	1.6 (1.53 – 1.68)	3.8
Simulation	43.3 (43.20 – 43.41)	1.7 (1.63 – 1.78)	3.9

*Values in parentheses denote the 95% confidence interval.

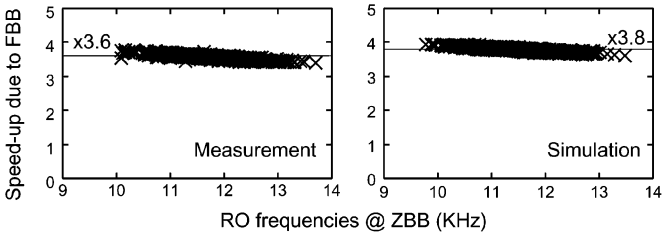


Fig. 24. Relation between 23-stage RO frequencies at ZBB and speed-up. Speed-up is defined as ratio of RO frequencies at FBB to those at ZBB.

NFACTOR at ZBB. Strictly speaking, the offset has a distribution; however, NFACTOR is the secondary effect as we mentioned in Section III-B and then NFACTOR that shifted uniformly is given to the simulation for simplicity.

Table VIII compares the measured and simulated 23-stage RO frequencies at $V_{\rm DD} = 0.3$ V with 0.3-V FBB in a single chip. There were 1000 runs in the Monte Carlo simulation. The average frequency (μ) was estimated with 3.6% error which is considered a significant difference, and the variation (σ/μ) was almost the same. We surmised that the average difference was caused by the dependence of depletion capacitance on the body voltage, because FBB was not supported in the original model card given by the foundry.

Fig. 24 plots the measured and simulated RO frequencies in a single chip. The horizontal axis is the measured/simulated RO frequency at ZBB. The vertical axis is the speed-up due to FBB, which is defined as the measured/simulated RO frequency at FBB divided by the measured/simulated RO frequency at ZBB. The measurement results in Fig. 24 indicate that the speed-up by slow ROs is larger than that of fast ROs, and the trend is well reproduced by the simulation with deterministic body-bias effect modeling. The measurement results reveal that the RO frequency at FBB is 3.6 times higher than that at ZBB when $V_{\rm DD} = 0.3$ V. In the simulation results, FBB multiplies RO frequencies by 3.8. The speed-up thanks to FBB is accurately estimated, even though there is an offset. We assume this is because the increase in depletion capacitance in the body was not considered in the simulation, and then the speed-up was overestimated in the simulation, which is similar to the situation in Table VIII.

We concluded that deterministic modeling of $V_{\rm th}$ shift due to body biasing provides accurate estimates of RO-frequency variations.

V. CONCLUSION

We evaluated the correlation between the variation model in the transistor-model card and ring-oscillation frequency as a primary metric of circuit performance. To characterize variations in subthreshold circuits, we designed a device-array circuit, and measured the variations in MOSFET I-V characteristics and RO frequencies. We demonstrated that modeling variations in I-V characteristics with $V_{\rm th}$ and subthreshold swing parameter n could be used to accurately estimate delay variations in subthreshold circuits.

We also examined the $V_{\rm th}$ shift due to body biasing. We revealed that $V_{\rm th}$ shift due to body-bias can be deterministically modeled with the analytical body-bias effect model. Our measurements also established that the body-bias effect depends on the temperature and gate width. We demonstrated that the deterministic body-bias model could accurately estimate the delay variations in subthreshold circuits with FBB.

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Hiroshi Fuketa (S'07) received the B.E. degree from Kyoto University, Kyoto, Japan, in 2002 and the M.E. degree in information systems engineering from Osaka University, Osaka, Japan, in 2008. He is currently pursuing the Ph.D. degree from the Graduate School of Information Science and Technology, Osaka University.

His research interests include ultra-low-power circuit design and variation modeling.

Mr. Fuketa is a student member of IEICE.

Masanori Hashimoto (S'00–A'01–M'03) received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively.

Since 2004, he has been an Associate Professor with the Department of Information Systems Engineering, Osaka University, Osaka, Japan. His research interests include computer-aided-design for digital integrated circuits, and high-speed circuit design.

Dr. Hashimoto was a recipient of the Best Paper Award at ASP-DAC 2004. He is a member of IEICE and IPSJ. He served on the technical program committees for international conferences including DAC, ICCAD, ASP-DAC, ICCD, and ISQED.

Yukio Mitsuyama (S'97–M'02) received the B.E. and M.E. degrees in information systems engineering from Osaka University, Osaka, Japan, in 1998 and 2000, respectively.

He is currently an Assistant Professor with Graduate School of Engineering, Osaka University. His research interests include reconfigurable architecture and its VLSI design.

Mr. Mitsuyama is a member of IEICE and IPSJ.

Takao Onoye (S'93–M'95–SM'07) received the B.E. and M.E. degrees in electronic engineering, and the Dr.Eng. degree in information systems engineering, all from Osaka University, Osaka, Japan, in 1991, 1993, and 1997, respectively.

He was an Associate Professor with the Department of Communications and Computer Engineering, Kyoto University, Kyoto, Japan. Since 2003, he has been a Professor in the Department of Information Systems Engineering, Osaka University. He has published more than 200 research papers in the field of VLSI design and multimedia signal processing in reputed journals and proceedings of international conferences. His current research interests include media-centric low-power architecture and its SoC implementation.

Dr. Onoye has served as a member of the CAS Society Board of Governors since 2008. He is a member of IEICE, IPSJ, and ITE-J.