All-Digital Ring-Oscillator-Based Macro for Sensing Dynamic Supply Noise Waveform

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***Abstract*—This paper proposes an all-digital measurement circuit called a "gated oscillator" to capture the waveforms of dynamic power supply noise. An improved gated oscillator with a power-gating structure is also proposed. The gated oscillator is constructed using standard cells, and thus is easily embedded in SoCs. Its performance was evaluated using test chips fabricated in a 90 nm process. The gated oscillator achieved 5.3–5.9 Gsample/s with an area of 10.08 $\times$ 6.72 μm^2, and the improved power gating structure achieved 6.6–8.3 Gsample/s in a 90 nm process. The characteristics of the gated oscillator and related design issues are also discussed. These characteristics were verified on silicon. We evaluated the effect of the decoupling capacitance based on measurement results obtained using the gated oscillator, and demonstrated that it could be used to verify power integrity.**

***Index Terms*—Decoupling capacitance, measurement circuit, power supply noise, ring oscillator.**

I. Introduction

POWER supply noise has become a serious problem in recent processes because of lower supply voltage and increased current consumption. Decoupling capacitance mitigates dynamic power supply fluctuations [1]–[4]. However, excessive decoupling capacitance consisting of MOS transistors results in severe gate leakage in advanced technologies[2], [5]. Though ensuring that adequate power supply wire also reduces power supply noise, wire resources are limited and excessive amount of power supply wire makes signal routing difficult. There are several studies on optimizing power distribution networks [6]–[12] based on simulation. However, these capacitance insertion and wire optimization methods are needed to be verified on silicon in terms of their noise suppression efficiency.

For this purpose, a small measurement circuit suitable for embedding in a device-under-test (DUT) is required to evaluate noise distribution within a chip. The simplicity of circuit and layout design is another important factor in probing various points of interest inside a chip. Existing measurement circuits [4], [13]–[23] use analog circuit techniques and need dedicated analog power and bias lines. The additional routing and area costs restrict the number of measurement circuits that can be integrated in a DUT and their allocatable positions. An ordinary ring oscillator measurement [24], which is easy to implement, observes the averaged supply voltage, not dynamic noise waveforms. The ring oscillator thus acquires limited information, and it cannot be used, for example, to evaluate the effects of decoupling capacitance.

In this paper, we propose an all-digital measurement circuit for dynamic noise waveforms, whose basic structure is described in our preliminary report [25], [26], and describe the validation of the operation of the proposed circuit on test chips. We also introduce an improved structure of the proposed circuit using power gating. In a previous report [22], a circuit for measuring dynamic noise waveforms using only digital circuit components was proposed. However, a limitation of this circuit is that the measurement system including the measurement circuit and a DUT has to synchronize with the clock generated inside the measurement circuit, and an external clock signal, which is often given from a phase-locked loop (PLL) or the outside of the chip, cannot be given to the DUT. As a result, the operation of the DUT is not freely changeable, and the flexibility of the measurement in terms of speed and intermittent operation is highly limited. On the other hand, when using the proposed circuit, any external clock can be supplied to the DUT, because the proposed circuit can operate synchronizing with the clock of the DUT. Our circuit has the following features: 1) it consists of only digital standard cells; 2) it does not require a dedicated analog power supply and reference voltage; 3) it has a small circuit area; and 4) it operates with any external clock.

These features are made possible by a new idea: the proposed circuit holds the ring oscillator state, whereas conventional circuits sample and hold the analog voltage[4], [14]. The proposed measurement circuit is very easy to implement because there is no need for the design techniques for analog circuits or for dedicated power lines for the measurement circuit. Our circuit can be built only using standard cells. Its layout design is compatible with common cell-based designs that use automatic placement and routing tools, and its size and shape are flexible. The operation clock of the DUT can be freely altered because our measurement circuit can synchronize with any reference clock given to the DUT.

We also discuss the characteristics of the proposed circuit and methods of improving its performance. The performance of the proposed circuit can be degraded by large slew of the transmission gate signal, unexpected charge accumulation, any kind of injection locking, and discharge of leakage current. We discuss

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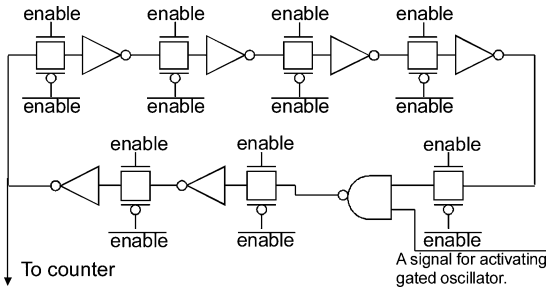

Fig. 1. Gated oscillator.

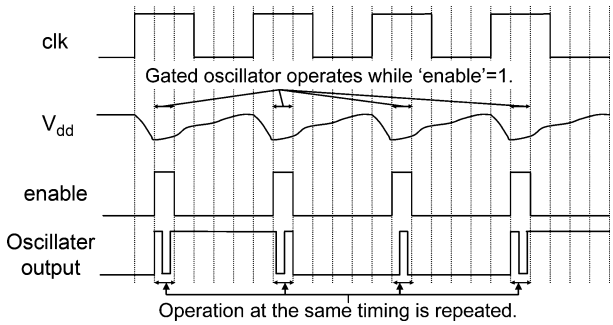

Fig. 2. Operation of gated oscillator.

the design features considering these characteristics The measurement results verified these characteristics and the improvement in performance.

In Section II, we explain the proposed measurement circuit. Section III describes the implementation of the test chips for evaluation of the proposed circuit. Section IV describes the evaluation of the proposed circuit on silicon, and Section V presents a case study on evaluating decoupling capacitance design using the proposed circuit. Section VI concludes this paper.

II. Proposed Circuit

This section describes the proposed measurement circuit for observing dynamic power supply noise. We also discuss the characteristics and performance improvement of the proposed circuit.

A. Basic Operation of the Proposed Circuit

Fig. 1 shows the proposed measurement circuit called a "gated oscillator," where the name derives from "gating" the ring oscillator by the transmission gates. The gated oscillator consists of only digital circuit components: inverters, a NAND gate, and transmission gates. The layout design of the transmission gate is simple, and the gated oscillator can basically be constructed using only standard cells though standard cell libraries do not necessarily include transmission gates.

The gated oscillator can observe dynamic waveforms of power supply noise. The operation of the gated oscillator is illustrated in Fig. 2. An ordinary ring oscillator can observe power supply voltage as a toggle count or frequency. However, it operates continuously and then measures only the average voltage over a long time period. Our new idea is introducing a state-keeping function to a ring oscillator. The gated oscillator operates only while 'enable' $= 1$, and the oscillating operation is stopped by the transmission gates when 'enable' $= 0$. A nonideality of the state preservation due to undesirable charge accumulation will be discussed in Section II-B. Suppose a power supply noise waveform in Fig. 2. The cycle count of the oscillator depends on only the power supply voltage while enabled. The supply waveform while 'enable'=1 is sampled, and the operation of the gated oscillator is hold while 'enable'=0. As a result, the analog voltage of the power supply noise at a specific timing is translated into a toggle count. To obtain a high enough toggle count for accurate measurement, the gated oscillator must be enabled repeatedly at the same timing. The repeated input of the same waveform is required as well as conventional sampling oscilloscopes.

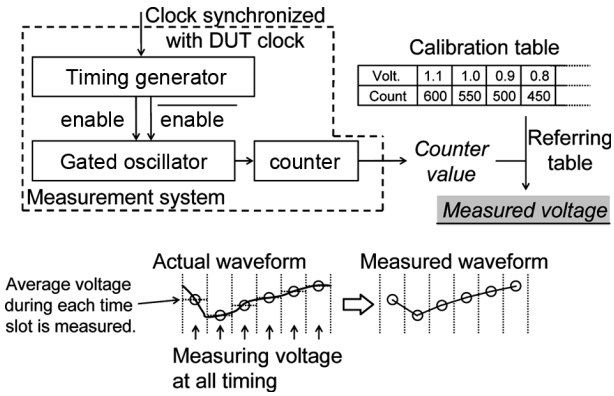

Fig. 3. Waveform measurement with gated oscillator.

We aquire the waveform from obtained toggle counts as shown in Fig. 3. The measured voltage is computed from the toggle count measured by the counter and the prepared calibration table. The calibration table describes the relation between the voltage and the toggle count, and is constructed beforehand by measuring the toggle count without any noise varying the voltage supplied to the proposed circuit. We repeatedly sweep the sampling timing using the timing generator, measure the count, and translate the count into voltage. The waveform is reproduced from the measured voltages at each timing as shown in Fig. 3. The measured voltage is the average voltage of the actual waveform during each time slot, and hence the bandwidth depends on the width of time slot in measurement.

The gated oscillator requires a simple digital counter, whereas conventional circuits need analog input/output or an analog-to-digital/digital-to-analog converter. In addition, common digital timing generators, which are often used in other sampling circuits, such as [14], [22], can be adopted for the timing generator of this circuit. Thus, the proposed measurement system can be easily embedded by using only digital standard cells.

The gated oscillator can be used to capture three waveforms; V_{dd} waveform, V_{ss} waveform, and V_{dd}–V_{ss} waveform. When the gated oscillator shares V_{dd} and V_{ss} with the DUT, it senses the V_{dd}–V_{ss} waveform, that is the voltage amplitude between V_{dd} and V_{ss}. On the other hand, when sharing V_{dd} (V_{ss}) only, the gated oscillator measures V_{dd} (V_{ss}) waveform.

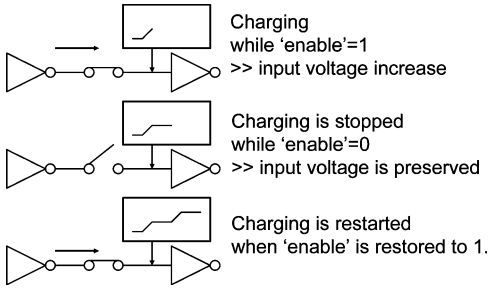

Fig. 4. Intermediate voltage preservation of gated oscillator.

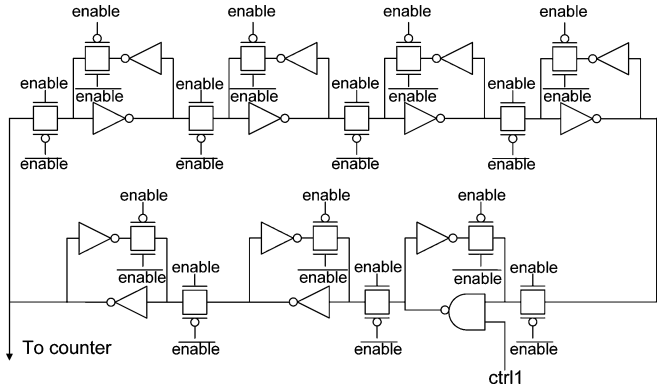

Fig. 5. Latch oscillator.

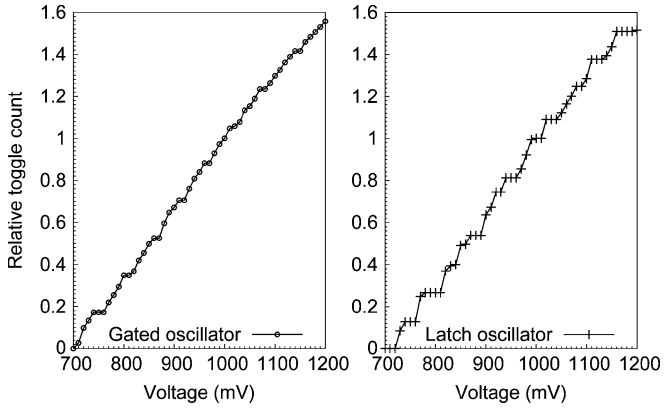

Fig. 6. Calibration table for gated and latch oscillators in simulation.

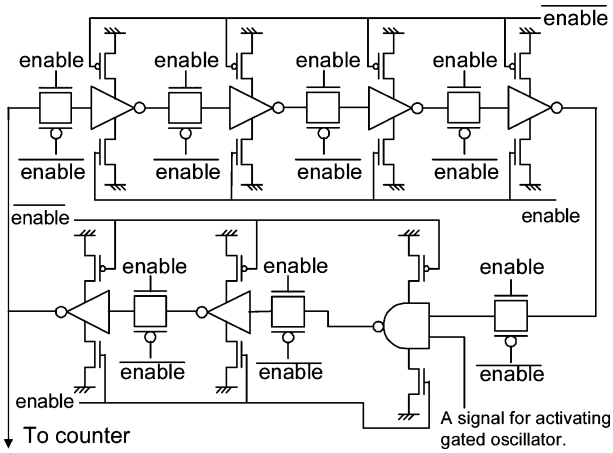

Fig. 7. Gated oscillator with power gating structure.

So far, for simplicity, the operation is explained supposing that the clock given to the DUT is also input to the timing generator. However, the gated oscillator can work even if the measurement timing is interleaved. Suppose that the same noise waveform is repeated every 10 clock cycles of the DUT as a simple example. In this case, by giving the clock divided by 10 to the gated oscillator, we can observe the noise waveform.

1) Intermediate Voltage Preservation and Power Gating Structure: An important metric of the measurement circuit is the voltage resolution. In the gated oscillator, the number of transmitting gates while 'enable' $= 1$ changes depending on the supply voltage.

In addition, our gated oscillator can preserve the intermediate voltage as shown in Fig. 4. When 'enable' is set from 1 to 0, charging or discharging next stage gate is stopped, and the gate input voltage is preserved at an intermediate level. After 'enable' is restored to 1, the transition restarts from the preserved intermediate level.

This intermediate voltage preservation improves the voltage resolution. Here we evaluate the improvement by circuit simulation. We use the gated oscillator and the "latch oscillator" shown in Fig. 5. The latch oscillator has feedback loops at each stage. In this structure, intermediate voltage preservation is disabled, and number of gate transmission while enable $=$ '1' is rounded to an integer value. Fig. 6 shows the simulated voltage resolution of two oscillators. The X-axis shows the stable supply voltage, and the Y-axis shows the toggle count of the gated oscillator normalized by the count at 1.0 V. The period and number of 'enable' $= 1$ are 300 ps and 250, respectively. The count increases linearly. Fig. 6 show that the toggle count of the oscillator is finely proportional to supply voltage, and as shown in Fig. 6 the gated oscillator is more sensitive to supply voltage than the latch oscillator. Thus, the intermediate voltage preservation improves the voltage resolution.

From the viewpoint of voltage preservation, we also propose an improved gated oscillator with a power gating structure as shown in Fig. 7. Two transistors for power gating are added for every inverter. The nMOS and pMOS for power gating are controlled by 'enable' signal for the transmission gates. This structure is more effective for voltage preservation, because charge sharing, which will be explained below, can be mitigated. Placing the customized inverter cells is as easy as placing standard cells though a custom layout is required for the inverter cells. The performance improvement provided by the power gating structure is discussed in detail in the next subsection.

2) Bandwidth: The bandwidth of the gated oscillator depends on the width of the 'enable' signal when the number of sampling points can be increased. This is because the average voltage is observed during the enable pulse. Here, we simulated the measurement operation of the gated oscillator using a sine waveform. Fig. 8 shows a simulation result of the measurement operation. The width of 'enable' was set to 200 ps. A 2 GHz sine waveform was fed to a gated oscillator, as shown in Fig. 8. Sampling with an 'enable' width of 200 ps was repeated every 50 ps. The gated oscillator finely observed the given sine

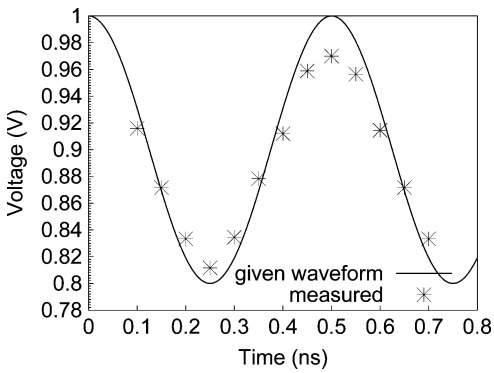

Fig. 8. Simulation result of measuring sine waveform with gated oscillator. Frequency of sine waveform was 2 GHz and 'enable' width was 200 ps.

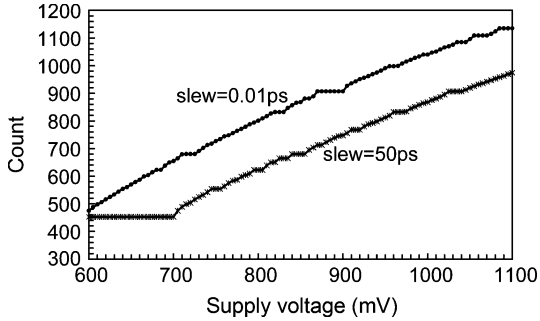

Fig. 9. Performance of transmission gate limits performance of gated oscillator (simulation).

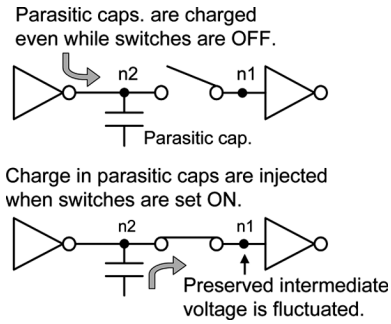

Fig. 10. Charge sharing.

waveform. In contrast, the measured waveform was attenuated when a high frequency sine waveform was observed. This is because the gated oscillator observes the average voltage while 'enable' signal is asserted. Sine waveforms of 1, 2, 2.5, and 3.3 GHz were measured. The amplitudes of the measured waveforms were −0.25, − 1.01, − 1.81, and −4.03 dB, respectively. If the acceptable amplitude is −3 dB, the bandwidth in this case is about 3 GHz. To improve the bandwidth, the width of 'enable' pulse must be shortened to reduce the averaging effect.

B. Characteristics and Design Issues

The most fundamental factor limiting the performance of the gated oscillator is the performance of the nMOS and pMOS transistors because the proposed gated oscillator consists of CMOS inverters and transmission gates. A gated oscillator with a faster transistor could achieve a higher sampling rate. When the manufacturing technology advances and gate switching becomes faster, it should be possible to operate using a shorter 'enable' pulse. Thus, the sampling rate and bandwidth of the proposed gated oscillator will improve as the technology advances.

The following three factors are also important in the performance of the gated oscillator:

(1) the transition time of the 'enable' signal;
(2) undesirable charge accumulation (charge injection and charge sharing);
(3) leakage in transmission gates.

The transmission gates stop and release the gated oscillator, and faster switching of the transmission gates would improve the performance of the gated oscillator. Thus, faster 'enable' transition of the transmission gate is desirable. Fig. 9 shows the simulated voltage resolution of the gated oscillator, when different slews of the 'enable' signal are given. The curve with a slow slew (50 ps) shows a lower voltage resolution than the curve with an ideal slew (0.01 ps). The slew of the 'enable' signal can be shortened by using a large driver, and also smaller gates for the gated oscillator.

When transmission gates are set ON or OFF, there exist undesirable charge accumulation which we do not expect. These effects can degrade the performance of the gated oscillator. Causes for the undesirable charge accumulation are charge injection and charge sharing.

First we refer to charge injection. When the transmission gates are set to OFF, the gate input voltage is preserved at an intermediate level. However, charge injection causes variation in the preserved voltage and adversely affects the performance of the gated oscillator. Charge injection is normally alleviated by balancing the size ratio of the pMOS and nMOS of the transmission gates. However, this method does not necessarily improve the signal-propagation performance of the transmission gate, and may lower the performance of the gated oscillator. As smaller transmission gate injects a smaller charge, in our experiments, simply using smaller transmission gates reduced charge injection.

Charge sharing is explained in Fig. 10. While the transmission gates are OFF, charging node n1 is stopped and the voltage of n1 is preserved. However, node n2 has parasitic capacitances, and the transmission gates cannot stop charging node n2. When the transmission gates are set to ON, the charge in node n2 is injected to node n1, and the preserved voltage fluctuates. A gated oscillator with a power-gating inverter, which was described in the previous section in Fig. 11, alleviates charge sharing. Power gating prevents the parasitic capacitance from being charged, as shown in Fig. 11, and improves the waveform acquisition performance.

Here we demonstrate the effect of two approaches mentioned above; using smaller transmission gates and the power gating structure. The simulation results for voltage resolution are shown in Fig. 12. Ideal repetitive pulses with 100 ps width were used as the 'enable' signal, and toggle counts were observed with a supply voltage from 0.6 to 1.1 V, increasing in 5 mV steps. The count of the gated oscillator basically increased monotonically as the supply voltage increased. However, there

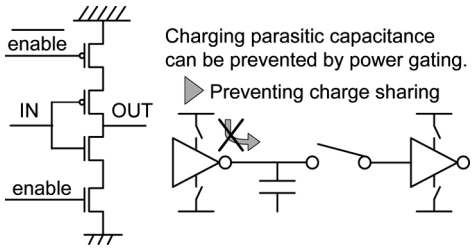

Fig. 11. Proposed power gating structure for gated oscillator.

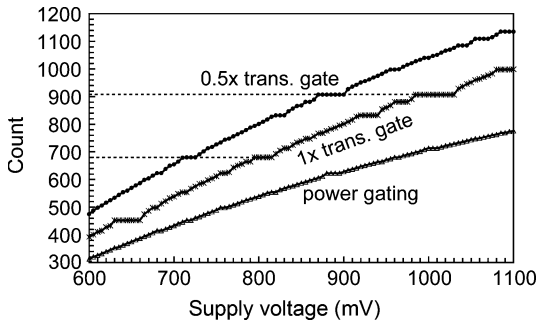

Fig. 12. Comparison of supply voltage vs. #toggles in simulation. Circuit structures differed and 'enable' was 100 ps wide.

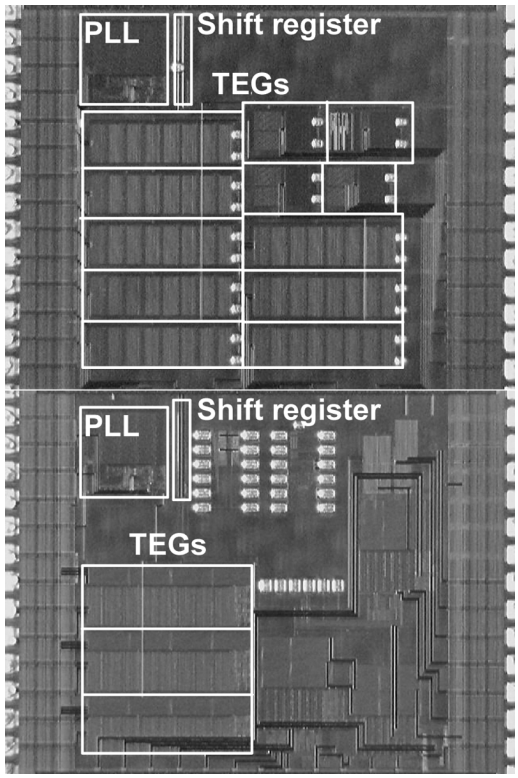

Fig. 13. Micrographs of two test chips.

were several voltage ranges where counts did not change. In this paper, we call this range the "insensitive voltage range." The small (0.5X size) transmission gate and power-gating inverter reduced the insensitive voltage range and improved the voltage resolution due to less charge injection and less charge sharing, respectively.

The insensitive voltage ranges are found at the same counts in structures with 1X and 0.5X transmission gates. For example, both structures have insensitive voltage ranges at counts of 680 and 907 in Fig. 12. In these cases, the enable widths are integral multiples of the stage delay of the gated oscillator, and the insensitive voltage ranges imply a kind of injection locking. In fact, 680 and 907 counts correspond to 25 ps and 33 ps gate delays that are 1/4 and 1/3 of the 'enable' width. The gated oscillator shows fine resolution at most voltage range other than insensitive voltage range. This range can be shifted by changing the configuration, i.e., the gate sizes, and sub-10-mV resolution can be achieved by implementing two differently configured gated oscillators.

When the transmission gates have a long OFF period, discharge due to leakage can also adversely affect the measurement results with the gated oscillator. The preserved intermediate voltage is not perfectly held because of the subthreshold leakage current in the transmission gate and the gate leakage current of the inverter. For example, supposing that the gate input capacitance and leakage current are 5 fF and 5 nA, respectively, for simplicity, and the preserved voltage is varied by 100 mV after a 100 ns holding period. Too long a holding period causes not only variation in the preserved voltage, but also functional failure. As mentioned in Section II-A, the gated oscillator works even when the measurement timing is interleaved. On the other hand, some design efforts might be required when the holding period would be long in a target measurement. In this case, transistors with low leakage current (e.g., high threshold voltage transistor) are likely to be selected for the transmission gates. Even if a low-leakage transistor is not available or not effective enough, the latch oscillator still works because its feedback structure maintains the condition of the oscillator.

III. Implementation of Test Chips

We fabricated two test chips using a 90 nm CMOS process. The nominal supply voltage of this process was 1.0 V. Fig. 13 shows micrographs of the test chips, which were 2.5×2.5 mm^2 in size. Each test chip included several TEGs, a PLL, and shift registers. The shift registers were written and read by external input and output. The control signals for the TEGs and PLL were stored in the shift registers. A part of the shift register also operated as a counter, and counted the toggles of the gated oscillator.

Each TEG included a DUT and a measurement circuit. The measurement circuit consisted of the gated oscillator and circuits for 'enable' signal generation. The external clock signal is input to DUTs as an operating clock. 'enable' signal is generated with given clock because 'enable' pulse needs to synchronizes with the given clock to observe waveform at the same timing repeatedly. Fig. 14 shows our 'enable' signal generator, which consists of variable delays, an XOR gate, AND gates, and a multiplexer. This generator varies the pulse width and timing of the 'enable' signal by controlling the variable-delay circuits. The generated pulse width is $|D1 - D2|$, where $D1$, $D2$ are the delays in the variable-delay circuits. The pulse timing of 'enable' from 'CLK' edge is changed from $\min(D1, D2)$ to $\max(D1, D2)$. The reference edge of 'CLK' is chosen from the rise and fall transition by the 'sel' signal. In this work, we used the variable delay circuit shown in Fig. 15, which consists

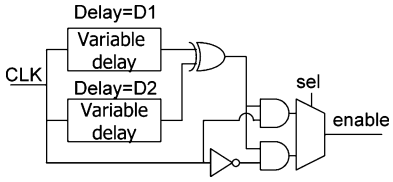

Fig. 14. Circuit for 'enable' signal generation.

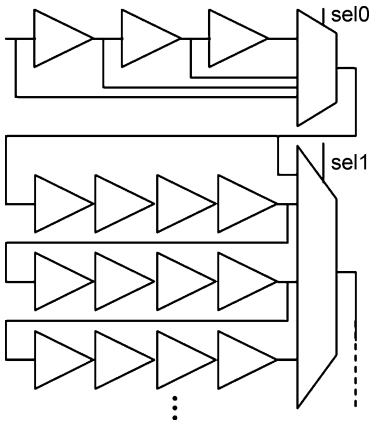

Fig. 15. Variable delay circuit.

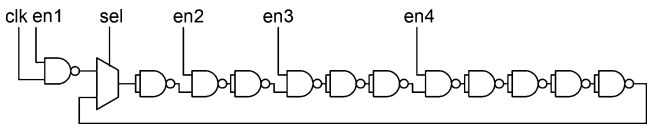

Fig. 16. Cell of noise source.

of buffers and multiplexers. $D1$ and $D2$ vary from 0-stage to 255-stage buffer delay.

The DUT includes switching circuits for noise generation, the power supply line, and decoupling capacitance. The noise-generation circuit consists of 12-stage NAND gates, as shown in Fig. 16. The number of operating stages can be controlled with 'en1'-'en4' signals. 64×8 cells of 12-stage NAND gates are placed in each TEG. Number of operating cells can also be selected from 0, 25, 50, 75, and 100% with the configuration stored in the shift registers. Each DUT has a dedicated external power supply directly connected to package pins, and the substrate of each DUT area is isolated by a triple-well structure. The power supply and ground of the gated oscillator are shared with the DUT, and the gated oscillator observes the power supply noise of the DUT. The power supply of the timing generator is separate from the DUT.

We implemented five configurations of gated oscillators and one configuration of a latch oscillator. Table I summarizes these configurations. 1X inverter consists of a 0.54-μm-wide nMOS and a 0.82-μm-wide pMOS. The nX inverter has n times larger nMOS and pMOS channel widths, respectively. The 1X transmission gate is composed of a 0.37-μm-wide nMOS and a 0.55-μm-wide pMOS. The 4X transmission gate has a 0.33-μm-wide nMOS and a 0.50-μm-wide pMOS. A power gating inverter adopts 3.36-μm-wide $(0.42\ \mu\text{m} \times 8)$ nMOSs and 5.12-μm-wide pMOSs $(0.64\ \mu\text{m} \times 8)$. Drawn channel length of all MOS transistors is 100 nm. The basic configuration $(\mathsf{G}_{\mathsf{basic}})$ is implemented in the first chip. This

TABLE I
CONFIGURATIONS OF IMPLEMENTED GATED OSCILLATORS AND LATCH OSCILLATOR

Name	Configuration
$\mathsf{G}_{\mathsf{basic}}$	4X inverters and transmission gates. 64X 'enable' driver.
$\mathsf{L}_{\mathsf{basic}}$	Latch oscillator. 4X inverters and transmission gates. 64X 'enable' driver.
$\mathsf{G}_{\mathsf{double}}$	8X inverters and 4X transmission gates. 128X 'enable' driver.
$\mathsf{G}_{\mathsf{balance}}$	Based on $\mathsf{G}_{\mathsf{double}}$. PN ratio of transmission gate is adjusted for charge injection.
$\mathsf{G}_{\mathsf{pgate}}$	Based on $\mathsf{G}_{\mathsf{double}}$. Power gating structure.
$\mathsf{G}_{\mathsf{small}}$	2X inverters and 1X transmission gates (Smallest implementation). 128X 'enable' driver.

configuration was designed for validation of gated oscillator operation. The inverters and transmission gates were 4X in size, and the ring oscillator had 11 stages. We did not use minimum-size gates to avoid unexpected process variations. The driver of the 'enable' signal was 64X corresponding to a 0.69 fan-out. The latch oscillator $\mathsf{L}_{\mathsf{basic}}$ was also implemented using the same configuration as the first chip, and we observed the impact of intermediate voltage preservation. The inverters and transmission gates for feedback operation were 1X in size.

The second chip included four configurations of the gated oscillator. Configuration $\mathsf{G}_{\mathsf{double}}$ consisted of 8X size inverters and 4X size transmission gates; the transmission gates were smaller than the inverters. The driver of 'enable' signal is strengthened to 128X, which corresponds to a 0.34 fan-out to shorten the slew of the 'enable' signal. The following configurations, $\mathsf{G}_{\mathsf{balance}}$, $\mathsf{G}_{\mathsf{pgate}}$, and $\mathsf{G}_{\mathsf{small}}$ were based on $\mathsf{G}_{\mathsf{double}}$. In Configuration $\mathsf{G}_{\mathsf{balance}}$, the ratio of the size of the nMOS to the pMOS in transmission gates was adjusted to reduce charge injection. The proposed power-gating structure was implemented in Configuration $\mathsf{G}_{\mathsf{pgate}}$ using the customized power-gating inverter cell shown in Fig. 11. Configuration $\mathsf{G}_{\mathsf{small}}$ included 2X-size inverters and 1X-size transmission gates, and was the smallest implementation. The layout size of $\mathsf{G}_{\mathsf{small}}$ was $10.08 \times 6.72\ \mu$m, which is similar or even smaller to the size of the other analog measurement circuits [4], [19].

IV. EVALUATION OF PROPOSED CIRCUIT ON TEST CHIPS

A. Validation of the Operation

Here, we describe the evaluation of the operation and measurement reproducibility of the proposed gated oscillator based on the measurement results with $\mathsf{G}_{\mathsf{basic}}$. The operation of the power-gating structure was also validated with $\mathsf{G}_{\mathsf{pgate}}$. The fabricated test chips were mounted on a QFP package. The external control signals were generated using a pattern generator, and the output signals, which included the gated oscillator counts, were observed using a logic analyzer.

Fig. 17 shows the measured cycle count of $\mathsf{G}_{\mathsf{basic}}$ and $\mathsf{G}_{\mathsf{pgate}}$ without noise generation, respectively. The widths of the 'enable' signal were about 400 ps $(\mathsf{G}_{\mathsf{basic}})$ and 140 ps $(\mathsf{G}_{\mathsf{pgate}})$. The X-axis shows the supply voltage, and the Y-axis shows the cycle count of the gated oscillator. The cycle count was measured for each 10 mV from 0.6 to 1.1 V. The relation between the cycle count and supply voltage increased monotonically, and the voltage resolutions were about 10–20 mV. The noise waveform was measured 1000 times to evaluate the reproducibility. The maximum standard deviation of $\mathsf{G}_{\mathsf{basic}}$ at 10 timing points

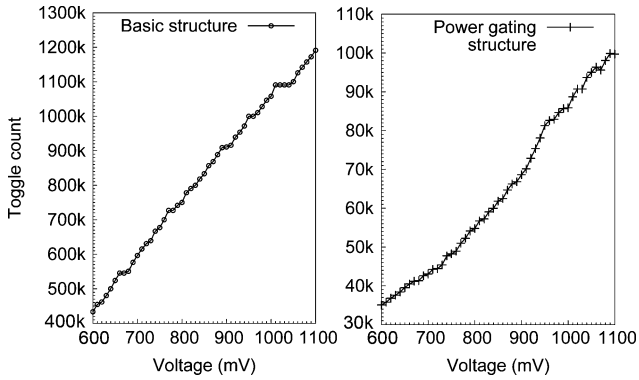

Fig. 17. Calibration results for gated oscillators with basic and power-gating structures (measured).

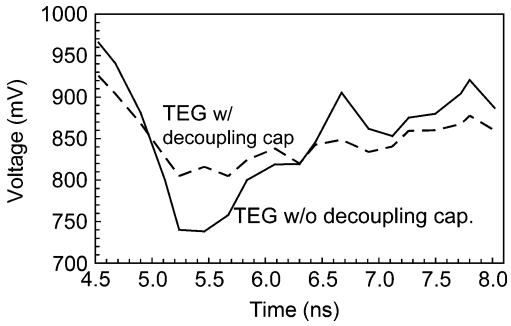

Fig. 18. Measurement results of TEGs w/ and w/o decoupling capacitance with G_{basic}. Inserted capacitance was 86.6 pF (the same area as noise source).

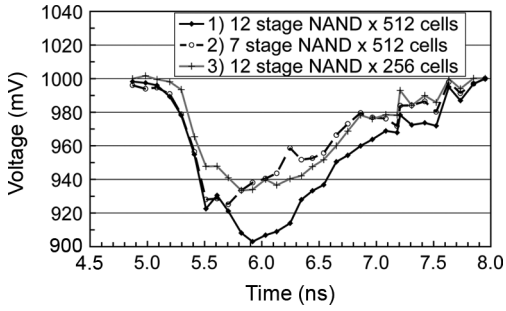

Fig. 19. Waveforms measured by gated oscillator with power-gating structure. Switching of (2) finished earlier than (1), and voltage recovery also occurred earlier in (2) than (1). As there were more switching cells, peak drop of (1) was larger than that of (3).

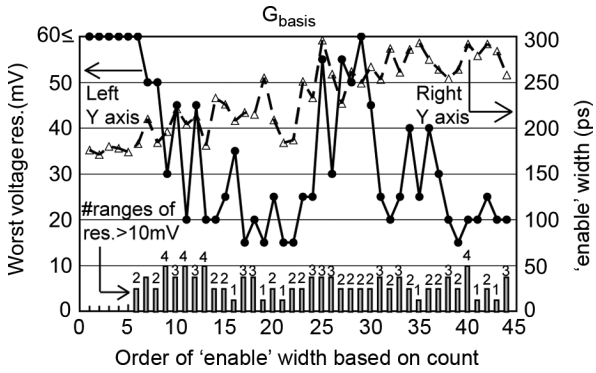

Fig. 20. Widths of 'enable' signal and poorest voltage precision in measurement results for G_{basic}. 'enable' width is time length of sampling pulse and corresponds to sampling rate.

was 0.98%, indicating that the gated oscillator had good reproducibility.

Fig. 18 shows the measured waveform using G_{basic} on the test chip. We measured the supply waveforms of two DUTs with and without decoupling capacitance with G_{basic}. The gated oscillator shared V_{dd} and V_{ss} with the DUT, and the amplitude of the power supply was measured. The area of inserted decoupling capacitance was the same as the noise source circuit. The measurement results for G_{basic} showed a clear difference between the two DUTs, and the waveform measured by the gated oscillator was found to be adequate.

We measured the supply noise waveforms at three different settings of the 12-stage NAND gate cells with G_{pgate}: 1) 12 stages, 100% cells operating; 2) 7 stages, 100% cells operating, and 3) 12 stages, 50% cells operating. Here, we connected the V_{dd} of the DUT to G_{pgate} and dedicated a clean V_{ss} line to the V_{ss} of the gated oscillator, and observed the V_{dd} waveform of the DUT. Fig. 19 shows the waveforms measured by G_{pgate}. The results indicate that (1) caused a larger peak drop than (3). Compared to (1), the voltage recovery started earlier in (2), because the switching of the noise generator finished earlier. These results are reasonable. Thus the operation of the power-gating structure was been validated from the measurement results of the cycle counts and waveforms.

B. Performance Evaluation

This section describes the measurement of the achievable sampling rate and voltage resolution of the implemented gated oscillators. Design issues related to improving performance of the gated oscillators were also evaluated.

Figs. 20–24 show the measurement results for voltage resolution with G_{basic}, G_{double}, $G_{balance}$, G_{pgate}, and G_{small}, respectively. These figures include two plots in solid and dashed lines and a histogram with labeled bars, and we here explain them in this paragraph. Each figure shows the poorest voltage resolution with solid circles and lines, where the corresponding axis is the left Y-axis. The poorest voltage resolution is the longest insensitive voltage range in the calibration result as shown in Fig. 17. The number of the insensitive voltage ranges larger than 10 mV is depicted at the bottom with the labeled bars. In this evaluation, toggle counts were measured at every 5 mV from 0.6 to 1.1 V. The frequency of the 'enable' pulse was 100 MHz and it was given 1,000,000 times at each measurement. The X axis means the configuration number of the enable pulse generation. The 'enable' width, that is, the time resolution, changed from 170 to 300 ps in Fig. 20, 80 to 270 ps in Figs. 21–24, and 160 to 320 ps in Fig. 22. The actual 'enable' width, which we wanted to know, could not be directly measured but was estimated in two ways. We first estimated it based on the measured delay values of the delay cells embedded in the 'enable' generator. These measured values are plotted in the dashed lines with the scale given by the Y-axis on the right. The 'enable' width was also estimated based on the count of the gated oscillator, and all measurement results explained above were plotted in the order of the estimated width. Thus, the smaller configuration number in the X-axis is expected to correspond to the shorter width of the enable pulse.

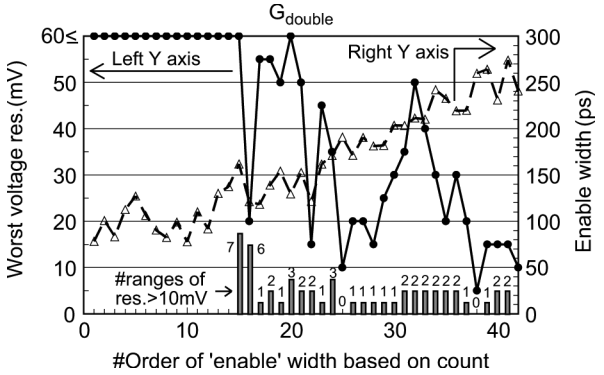

Fig. 21. Widths of 'enable' signal and poorest voltage precision in measurement results for G_{double}. 'enable' width is time length of sampling pulse and corresponds to sampling rate.

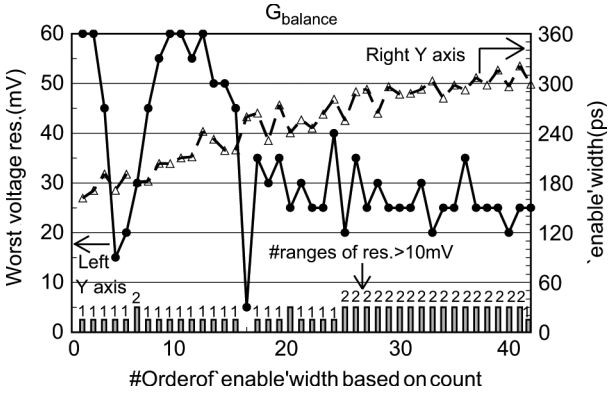

Fig. 22. The widths of 'enable' signal and poorest voltage precision in measurement results for $G_{balance}$. 'enable' width is time length of sampling pulse and corresponds to sampling rate.

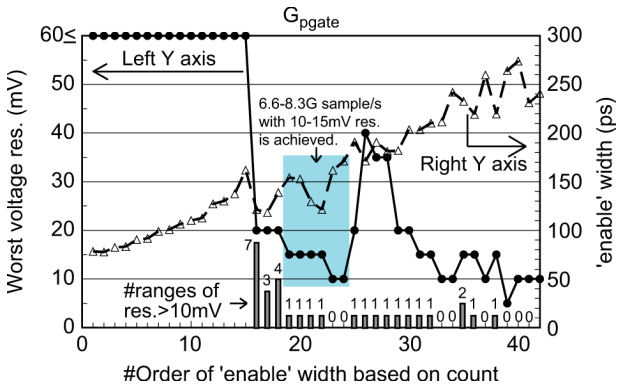

Fig. 23. The widths of 'enable' signal and poorest voltage precision in measurement results for G_{pgate}. 'enable' width is time length of sampling pulse and corresponds to sampling rate.

G_{basic} has 15–20 mV voltage resolution with 200–250 ps time resolution (no. 17–24 on X-axis) in Fig. 20. A few insensitive voltage ranges were also observed. The insensitive voltage ranges of 30–50 mV appear at a time resolution of about 250 ps (no. 25 to 30). As discussed in Section II-B, a type of locking may cause this deterioration in performance.

G_{double} has 10–20 mV voltage resolution with about 180 ps a time resolution (no. 25–28 on X-axis) in Fig. 21. The number of insensitive voltage ranges observed was one or zero. We adjusted the slew of the 'enable' signal and gate sizes in G_{double}.

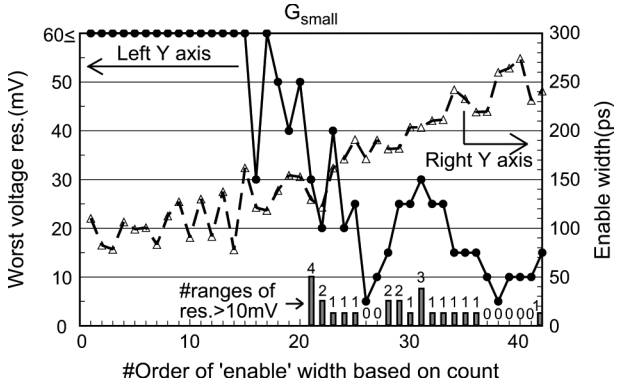

Fig. 24. Widths of 'enable' signal and poorest voltage precision in measurement results for G_{small}. 'enable' width is time length of sampling pulse and corresponds to sampling rate.

The measurement results show that the voltage resolution and sampling rate can be improved by incorporating these design considerations.

A voltage resolution of about 25 mV with an 'enable' width of 240–300 ps was observed for $G_{balance}$. This configuration did not improve the performance of the gated oscillator because the signal-propagation performance of the transmission gate was degraded by adjusting the PN ratio considering only charge injection.

G_{pgate} achieved a voltage resolution of 10–15 mV with a time resolution 120–150 ps (no. 19–24 on X-axis) in Fig. 23. The number of insensitive voltage ranges was also one or zero. The power-gating structure of the G_{pgate} improved the performance of the gated oscillator. G_{small} achieved voltage resolution of 5–25 mV with a time resolution of 170–190 ps (no. 24–29 on X-axis) in Fig. 24. This smallest implementation provided good voltage and time resolution.

G_{small} performed better than G_{double}. G_{double} and G_{small} were implemented in the same configuration. The inverters and transmission gates in G_{small} are one-quarter the size of those in G_{double}. The driver sizes of G_{small} and G_{double} were equal. The driver fan-out of G_{small} was larger than that of G_{double}, and the slew of the 'enable' signal in G_{small} was able to be shortened, which helped to improve the performance of G_{small}.

The features of G_{pgate} and G_{small} are summarized in Table II. G_{small} was implemented in the smallest area and achieved 5.3–5.9 Gsample/s compared to the other gated oscillators implemented. G_{pgate} showed the highest voltage resolution and sampling rate in this paper, and the layout size on the test chip was $12.60 \times 16.24\ \mu m^2$. As G_{double} could be shrunk to G_{small} without reducing its performance, G_{pgate} was also able to be implemented with smaller gates. When 2X inverters (power-gating structure) and 1X transmission gates are used, the layout size of G_{pgate} can be scaled to $10.08 \times 9.24\ \mu m^2$.

C. Discharging Effect and Latch Oscillator

As discussed in Section II-B, the gated oscillator cannot hold its state when there is a long holding period and a large leakage current in the transistors.

Fig. 25 shows the results of measuring the relation between the supply voltage and the cycle count of G_{basic} and L_{basic}. The width and frequency of the 'enable' signal were set to 800 ps and

TABLE II
PERFORMANCE OF TWO GATED OSCILLATOR STRUCTURES: SMALLEST DESIGN AND POWER-GATING STRUCTURE

		Gated oscillator with smallest cells (G_{small})	Power gating structure (G_{pgate})
Sampling rate (15mV resolution)		5.3-5.9G sample/s	6.6-8.3G sample/s
Area (μm^2)	Test chip	10.08×6.72	12.60×16.24
	Smallest design	10.08×6.72	10.08×9.24
Required cells		standard cells	standard & custom cells
Compatibility with cell-based design		YES	YES

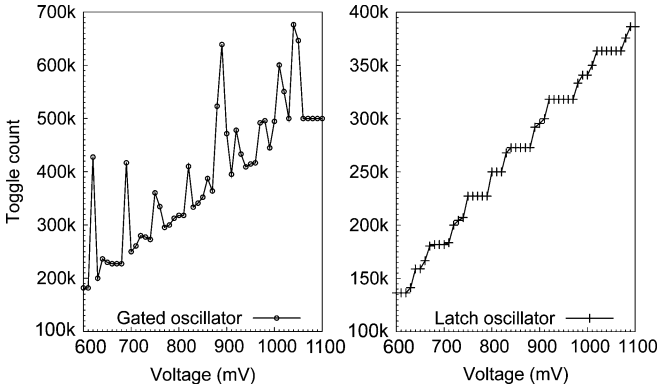

Fig. 25. Calibrations of G_{basic} and L_{basic} in measurement using 800 ps 'enable' width, and 1.56 MHz 'enable' signal frequency.

1.56 MHz, respectively. As shown in the left of Fig. 25, spikes in the cycle counts were observed at several voltages. These spikes are a deterministic phenomenon, and their reproduction was observed at several measurement times. The supply voltage cannot be calculated from the measured cycle count as the gated oscillator cannot hold its state. In contrast, the cycle count of the latch oscillator increased in proportion to the supply voltage, as shown in the right of Fig. 25. The latch oscillator has a feedback structure, and its functionality is not reduced by leakage current in transmission gates. However, as can be seen, the voltage and time resolution were inferior to those of the gated oscillators because the latch oscillator cannot preserve the intermediate voltage. However, the latch oscillator may be useful in an intermittent operation.

V. APPLICATION OF GATED OSCILLATORS

A gated oscillator observes the dynamic waveform of power-supply noise, and can be used to verify the design of a power-supply network. In this section, we examine the use of a gated oscillator to validate the characteristics of decoupling capacitance. The TEGs measured in this section were implemented on the first chip, and G_{basic} was used for the measurement.

A. Evaluation Setup

Below, we discuss the effect of decoupling capacitance (decap) focusing on the channel length and resistance between the operating circuit and capacitors. The structure of the DUT in each TEG is shown in Figs. 26, 27 and variation in TEG are summarized in Table III. We changed the channel length of the decoupling capacitance so that the area or the total capacitance

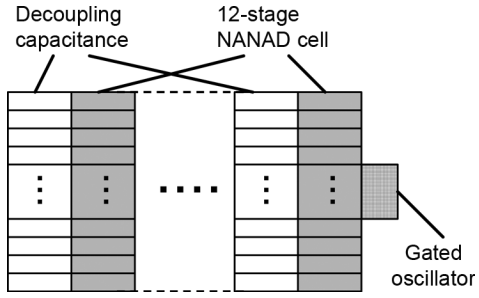

Fig. 26. Structure of DUT for TEG A-D.

TABLE III
DUT CONFIGURATIONS OF TEGS

TEG	Decap ch. length	Note
A	-	No decap
B1	0.1 μm	Decap capacitance is same as TEG C.
B2	0.1 μm	Decap area is same as TEG C.
C	1 μm	86.6 pF (the same area as noise source)
D1	5.98 μm	Decap capacitance is same as TEG C.
D2	5.98 μm	Decap area is same as TEG C.
E	1 μm	Wire R is 1.7 Ω. Decap is same as TEG C.
F	1 μm	Wire R is 26.7 Ω. Decap is same as TEG C.

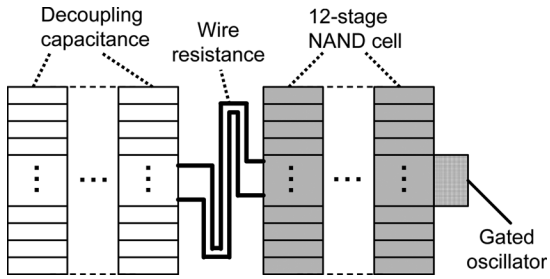

Fig. 27. Structure of DUT for TEG E and F.

would remain unchanged (TEG B-D). The resistance to the decoupling capacitance was varied in TEG E and F. Wire resistance was inserted into the power supply for TEG A-D to damp the package-inductance effect and to protect the device from being destroyed by voltage overshoot.

The cycle of the gated oscillator was measured five times under the same condition and the average of five values was used to compute the voltage computation. The pulse of the gated oscillator was counted for 20 ms, and 'enable' signal was generated for every 10 ns.

TEG A was used to demonstrate the noise-reduction effect of inserting decoupling capacitance. The measured peak-voltage drop with TEG A was 70 mV larger than TEG C, which included 86.6-pF decoupling capacitance, as shown in Fig. 18.

B. Channel Length of Decoupling Capacitance

We first discuss the channel length of the decoupling capacitance. Fig. 28 compares the noise in TEG B1 ($\mathrm{L} = 0.1\ \mu\mathrm{m}$), TEG C ($\mathrm{L} = 1\ \mu\mathrm{m}$), and TEG D1 ($\mathrm{L} = 5.98\ \mu\mathrm{m}$). The Y-axis in Fig. 28 shows the voltage difference between V_{dd} and V_{ss}. The total capacitance values of the decoupling capacitors in the three TEGs were almost equal. The peak-voltage drop of TEG D1 was 20 mV larger than those of other TEGs, which indicates that a long channel length degrades the RC time constant of the

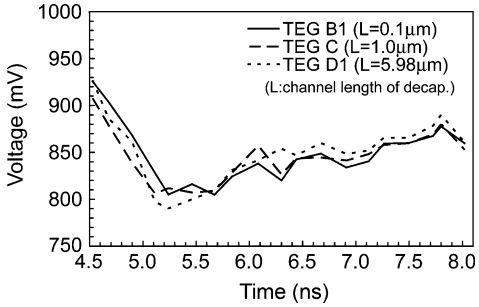

Fig. 28. Measurement results for TEGs with 0.1(B1)/1(C)/5.98(D1)μm. Total capacitance of decoupling capacitance was almost equal.

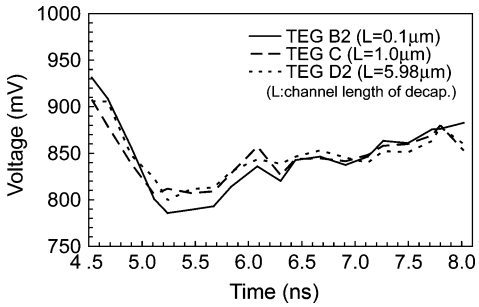

Fig. 29. Measurement results for TEGs with 0.1(B2)/1(C)/5.98(D2)μm channel-length decoupling capacitance. Area of capacitors was equal.

decoupling capacitance. Even if all the inserted decoupling capacitance was removed, the peak-voltage drop increased only 70 mV, and this 20 mV increase in the voltage drop is remarkable. In contrast, the peak-voltage drop of TEG B1 and C were almost the same, though the channel length was different. In this case, we consider that the RC time constant of L = 1 μm decap was small enough for noise suppression.

Next, we kept the decap area unchanged for different channel lengths, and compared the noise (Fig. 29). Generally, a larger capacitance can be integrated into the same area by using longer channel transistors. The ratio of the total capacitance among the TEGs is about B2:C:D2 = 2:6:9. The peak-voltage drop of TEG B2 was larger because of the small total capacitance. A similar result was observed in TEG C and D2. Though TEG D2 had 1.5 times more capacitance than TEG C, the voltage drop did not decrease because of the poor RC time constant.

This measurement result indicates that using decoupling capacitance with an appropriate channel length can improve the area efficiency without degrading the effect of noise suppression. However, when the channel length is too long, the performance of the decoupling capacitor deteriorates. Thus, the characteristics of decoupling capacitance, from the viewpoint of channel length, were validated using the proposed gated oscillator.

C. Resistance Between Operating Circuit and Decoupling Capacitance

Fig. 30 compares the measured supply noise waveforms of TEGs E and F. The resistance difference between the operating circuit and decoupling capacitance (1.7 Ω and 26.7 Ω) corresponded to the difference in the distance from the decoupling

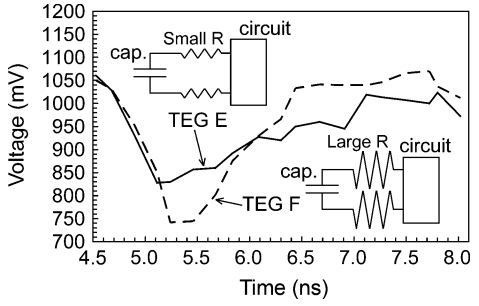

Fig. 30. Measurement results for TEGs E and F. Wire resistances between operating circuit and decoupling capacitance of TEGs E and F were 1.7 and 26.7 Ω, respectively.

capacitance in the actual designs (16 μm and 250 μm). The difference in the peak-voltage drop between the two TEGs was about 80 mV. We found that wire resistance degraded the RC time constant for the decoupling capacitance and noise-suppression effect. The resistance/distance from the decoupling capacitance must be carefully examined to avoid unexpected large noise. Consequently, the proposed gated oscillator clearly observed the impact of the distance between the decoupling capacitance and the operating circuit.

VI. Conclusion

We proposed an all-digital gated oscillator that captures dynamic supply-noise waveforms. The gated oscillator does not directly capture analog voltage, but involves a new concept based on holding the ring oscillator state. The gated oscillator ignores voltage fluctuations during the holding period, and senses the supply voltage during the activated period. The noise waveform is reproduced from the measured cycle of the ring oscillator. The gated oscillator consists only of digital standard cells, and does not require analog circuits dedicated power lines and reference voltage. The physical design of the gated oscillator is simple and compatible with cell-based design, and the shape of the measurement circuit is flexible and can be changed. We discussed the characteristics of the gated oscillator, and the proposed power-gating structure and improvements to the performance of the gated oscillator.

The operation of the gated oscillators with both a basic structure and a power-gating structure were validated on test chips fabricated using a 90 nm CMOS process. We found that the cycle count of the gated oscillator increased in proportion to the supply voltage, and that the supply voltage could be calculated from the measured cycle count. The waveforms measured with the gated oscillators were qualitatively consistent with the configurations of the noise sources. We evaluated the performance of various gated oscillators implemented on test chips. A gated oscillator with a power-gating structure achieved 6.6–8.3 Gsample/s with a voltage resolution of 10–20 mV, and 5.3–5.9 Gsample/s with an area of 10.08 $\times$ 6.72 μm^2. The characteristics of the gated oscillator and related design issues were also verified through measurement. As an example of potential applications, we evaluated the characteristics of decoupling capacitance on silicon. The gated oscillator clearly demonstrated differences in noise reduction depending on the characteristics of the decoupling capacitance design.

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