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Improvement in Computational Accuracy of Output Transition Time Variation Considering Threshold Voltage Variations****

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SUMMARY Process variation is becoming a primal concern in timing closure of LSI (Large Scale Integrated Circuit) with the progress of process technology scaling. To overcome this problem, SSTA (Statistical Static Timing Analysis) has been intensively studied since it is expected to be one of the most efficient ways for performance estimation. In this paper, we study variation of output transition-time. We firstly clarify that the transition-time variation can not be expressed accurately by a conventional first-order sensitivity-based approach in the case that the input transition-time is slow and the output load is small. We secondly reveal quadratic dependence of the output transition-time to operating margin in voltage. We finally propose a procedure through which the estimation of output transition-time becomes continuously accurate in wide range of input transition-time and output load combinations.

key words: *SSTA, output, transition time, gate delay model, process variation*

1. Introduction

Statistical static timing analysis (SSTA) [4]–[6], [8] has been studied extensively to efficiently cope with increasing process variation [9] due to process technology scaling. In contrast to conventional static timing analysis (STA) that uses the best and the worst corner conditions, SSTA directly propagates statistical parameters of delay variation. It is expected to eliminate excess timing margins existing in the conventional STA.

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In timing analysis used for the SSTA, a statistical gate delay model and delay calculation, which calculates pin-to-pin propagation delay and output transition-time according to given input transition-time and output load, are necessary. So far, the output transition-time has not been studied earnestly since the impact of the output transition-time on delay is considered as a secondary effect. Most works have focused on the calculation of propagation delay.

To the best of our knowleadge, studies on statistical analysis of the output transition-time are as follows. Chang, et al. proposed first-order sensitivity-based approach in [1]. It is only mentioned that the output transition-time variation can be treated in the same way as the delay variation but no example has been given in the literature. Gavial, et al. reported accuracy improvement of the estimation of output transition-time variation by extending the first-order sensitivity-based approach to consider the propagation of transition-time in [2]. Kouno, et al. observed a high correlation between delay and output transition-time and exploited it to estimate the output transition-time variation [3]. However, as mentioned in the same reference, the correlation does not become high enough in certain combinations of input transition-time and output load. References [2] and [3] do not mention how to cope with the low correlation cases.

In this paper, we focus on the low correlation conditions where the existing works have ignored. We newly point out that the threshold voltages of both PMOS and NMOS transistors affect the output transition-time in those cases as opposed to the high correlation cases where the threshold voltage of either PMOS or NMOS transistor have dominant influence. We also show that output transition-time in the low correlation cases has predictable quadratic dependence on the voltage margin that is defined by using threshold voltages of both types of transistors. From the above observations, an equation that improves estimation accuracy of output transition-time variations will be proposed.

The rest of the paper is organized as follows. In Sect. 2, we experimentally study the variation of output transition-time and show that existing first-order sensitivity-based approach is valid only in the cases that the delay and output transition-time are linearly correlated. In Sect. 3, we examine how the threshold voltages of PMOS and NMOS transistors affect the output transition-time in the lower correlation cases. In Sect. 4, we propose and evaluate a method

to estimate the output transition-time variation accurately under a wide range of input transition-time and output load combinations by combining the conventional first-order sensitivity-based approach and the observed quadratic relations. Section 5 concludes the paper.

2. Review of Conventional Method to Estimate the Output Transition-Time Variation

Figure 1 depicts our experimental circuit setup and input/output timing definitions. Correlation coefficients between 50% gate-delay and output transition-time are calculated under the conditions and the parameters summarized in Table 1. As shown in the table, we use threshold voltages of NMOS and PMOS transistors (V_{tn} and V_{tp}, respectively) as the source of variation. The variations are applied to each type of transistors independently. The correlation coefficients as functions of input transition-time ($t_{R,in}$) with various output load capacitances (C_L) are plotted in Fig. 2. From the figure, higher correlations are observed in the condition of small input transition-time and large output load as mentioned in [3]. However, there exist the cases where the coefficients become lower. In particular, combinations of large input transition-time and small output load result in small or negative correlations.

Figures 3 (a) and (b) show the distributions of delay and output transition-time in the high and the low correlation cases. The skewness/kurtosis of the delay distributions in Figs. 3(a) and (b) are 0.428/0.856 and 0.241/0.484 respectively. These values are less than 1.0, meaning that both distributions can be considered as the normal distribution. The output transition-time distribution in Fig. 3(a) also has skewness/kurtosis of 0.518/1.13, implying that the distribution can be also considered as nearly normal. In contrast, the distribution of output transition-time in Fig. 3(b) shows a positive skew (heavy tail in larger output transition-time) with skewness/kurtosis of 2.25/7.27. The distribution can not be treated as the normal any more. The cause of this deviation from the normal distribution will be discussed in detail in Sect. 3.

Figure 4(a) plots the output transition-time as functions of threshold voltages of NMOS and PMOS transistors in the case of high correlation. The falling transition-time has strong linear correlation with threshold voltage of NMOS transistor and seems to have no correlation with the

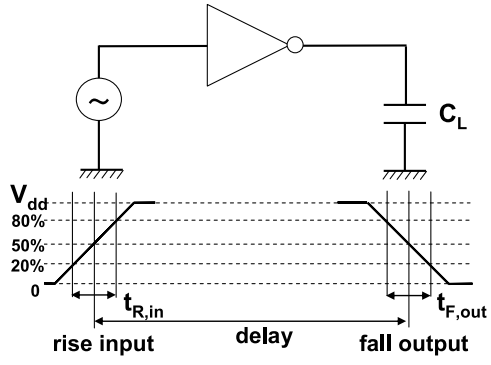

Fig. 1 Experimental circuit setup and timing definitions.

Table 1 Details of experimental conditions.

Tr.	Model	BSIM4
	Process	PTM 65nm, Typical [7]
	NMOS	L=60(nm), W=300(nm) V_{tn}=N(0.423, 0.03^2) (V)
	PMOS	L=60(nm), W=500(nm) V_{tp}=N(-0.365, 0.025^2) (V)
V_{dd}		1.0 (V)
temp.		25 (℃)
C_L		3, 10, 30, 50, 100 (fF)
$t_{R,in}$		20, 40, 60, 100 , 200 (ps)
Analysis Method		Monte-Carlo Analysis (1000 Times)
Simulator		Hspice [10]

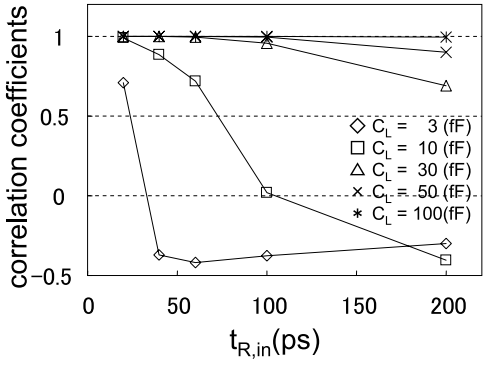

Fig. 2 Correlation coefficients between delay and output transition time under the combinations of input transition time ($t_{R,in}$) and output load (C_L) in Table 1.

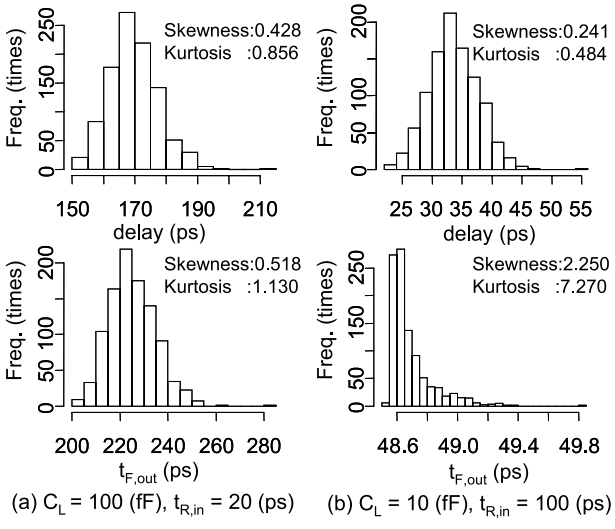

Fig. 3 Distributions of delay and output transition-time dependent on the correlation between delay and output transition-time: (a) High correlation combination case. (b) Low correlation combination case.

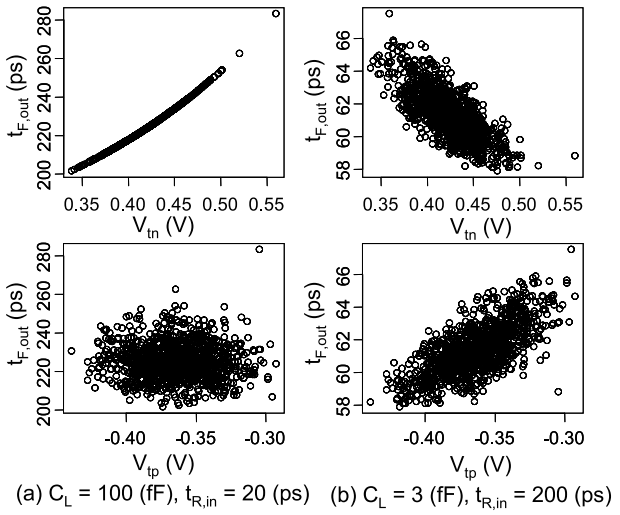

Fig. 4 Scatter plot of output transition-time and NMOS/PMOS threshold voltages dependent on the correlation between delay and output transition-time: (a) High correlation combination case. (b) Low correlation combination case.

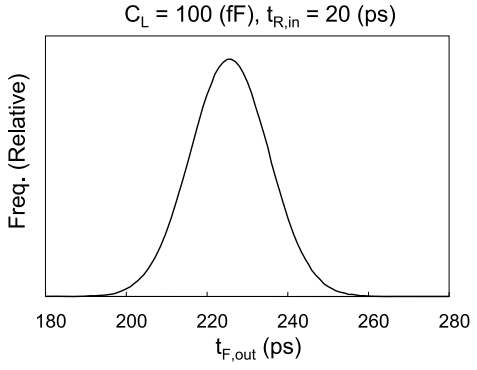

Fig. 5 Computed result of the output transition-time distribution by the approximated linear correlation in the high correlation case of Fig. 3(a).

one of PMOS transistor. From Figs. 3(a) and 4(a), it can be seen that NMOS threshold voltage mainly contributes to switching operation, resulting in the dominance of the output transition-time. Note that the linear correlation is observed in the cases of fast input transition-time and large output load. The discharge current through the NMOS transistor mainly forms output waveform, resulting in strong dependence of the output transition-time.

Figure 5 is the distribution of computed output transition-time under the conditions of Fig. 3(a) based on the linear correlation between NMOS threshold voltage and output transition-time $tsl1$ by the following equation.

$$tsl1 = \alpha \cdot V_{tn} + \beta \tag{1}$$

Here, α and β are the slope and the intercept of the linear correlation characteristics, respectively. The coefficients α, β are obtained through linear least squares method using the data plotted in Fig. 4(a). The output transition-time distribution in Fig. 5 is determined by linear projection using Eq. (1) being the normal distribution $N(0.423, 0.03^2)$ of the threshold voltage of NMOS transistor shown in Table 1 as the input.

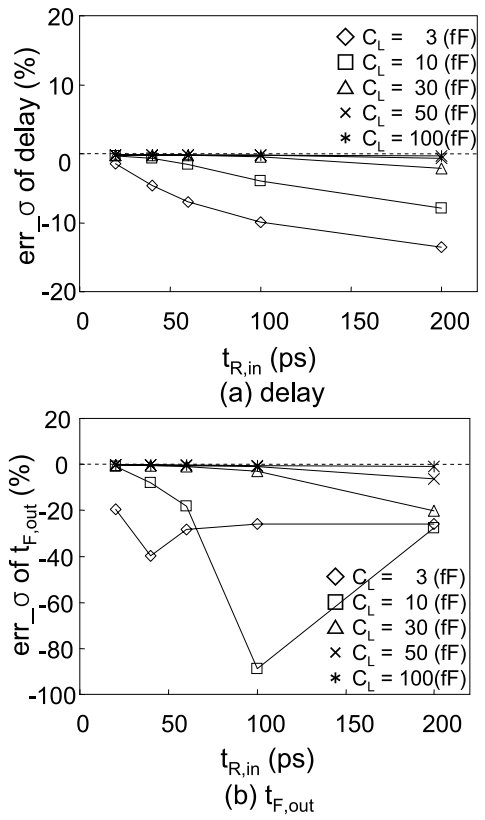

Fig. 6 err_σ (%) of the estimated distribution by the linear correlation of NMOS threshold voltage: (a) Delay time distribution. (b) Output transition-time distribution.

The shape of the distribution in Fig. 5 agrees well with the distribution of output transition-time shown in Fig. 3(a). The first-order sensitivity-based approach in [1] assumes the linear correlation around the mean value of variation parameters, which always results in similar distributions between input parameter and output transition-time variations.

Figure 6 plots the accuracies of estimated distribution of (a) delay and (b) output transition-time both by using Eq. (1). The variability error is defined as

$$err\_\sigma(\%) = \frac{\sigma_{est} - \sigma_{ref}}{\sigma_{ref}} \times 100. \tag{2}$$

Here, σ_{ref} and σ_{est} are the standard deviations of the reference Monte Carlo simulation result and estimated variation using Eq. (1), respectively. Input transition-time and output load combinations are varied according to the values listed in Table 1. The variability error in estimated delay distribution of Fig. 6(a) is 15% at the maximum, which proves the effectiveness of the first-order sensitivity-based approach. However, the variability error of the estimated output transition-time distribution in Fig. 6(b) exceeds 80% under the low correlation cases of slow input transition-time and small output load capacitance.

3. Detailed Analysis of the Skewed Distribution in Low Correlation Cases

Figure 4(b) shows the scatter plot between output transition-time and threshold voltages of NMOS/PMOS transistors in the cases of low correlation between delay and output transition-time. The figure shows that the output transition-time has negative correlation with NMOS threshold voltage and positive correlation with PMOS threshold voltage. It can be observed that the large output transition-time condition corresponds to the combinatorial condition of the low NMOS and high PMOS threshold voltages. Conversely, the small output transition-time condition corresponds to the combination of high NMOS and low PMOS threshold voltages. The above relationship can be more compactly summarized by the difference in threshold voltages between NMOS and PMOS transistors. Figure 7 plots the output transition-time of Fig. 3(b) using the following metric called voltage margin or operating margin in voltage.

$$V_{margin} = V_{dd} - |V_{tp}| - V_{tn} \tag{3}$$

Figure 7 shows clear relationship between the output transition-time and the V_{margin}. When the NMOS or PMOS threshold voltages are individually considered, no trend has been extracted as in Fig. 4(b). Note that the functional relationship can no longer be considered linear. Instead, we now see that the output transition-time has quadratic dependence on the V_{margin}. From now on, we will refer these characteristics as quadratic relation of voltage margin (or just a quadratic relation in short) and approximate the characteristics of output transition-time $tsl2$ using the following equation.

$$tsl2 = a(V_{margin} - x0)^2 - y0 \tag{4}$$

where a is the quadratic coefficient, $x0$ is the value of V_{margin} at which the output transition-time becomes the minimum and $y0$ is corresponding minimum value. Projection of threshold voltages on Eq. (4) determines the shape of transition-time distribution. When the center of V_{margin} variation is located about $x0$, the distribution of the output transition-time is expected to be truncated at $y0$. Figure 3(b) seems to be a good example of the projected distribution.

Figure 8 shows the computed output transition-time distribution using parameter variations in Fig. 3(b). Coefficients a, $x0$, and $y0$ are approximated through quadratic least square method using the data of Fig. 7. The V_{margin} variation is determined as the normal distribution $N(1 - 0.365 + 0.423, 0.025^2 + 0.03^2)$ based on NMOS and PMOS threshold voltage variations in Table 1. The shape of the distribution in Fig. 8 agrees well with the one in Fig. 3(b).

We investigated other combinations of input transition-time and output load capacitance, and confirmed that there always exists a quadratic relation between V_{margin} and output transition-time in low correlation cases. Figure 9 plots the variability error of computed output transition-time distribution by using Eq. (4) under the same combinations of input transition-time and output load capacitance in Fig. 6(b). Comparison of Figs. 9 and 6(b) shows the range of dominance of quadratic relation since low correlation cases in Fig. 2 are significantly improved while high correlation cases are deteriorated. Whether truncation is observed or not, the shape of distribution is determined by the rela-

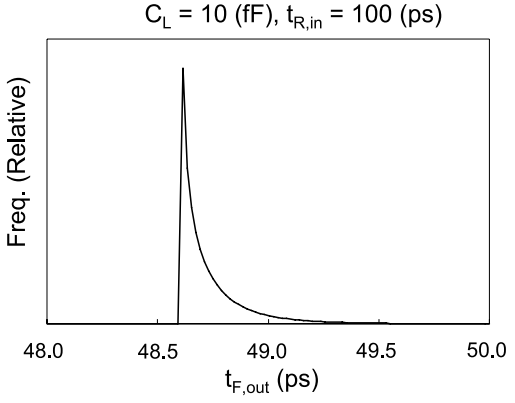

Fig. 8 Computed result of the output transition-time distribution by the approximated quadratic relation in the low correlation case of Fig. 3(b).

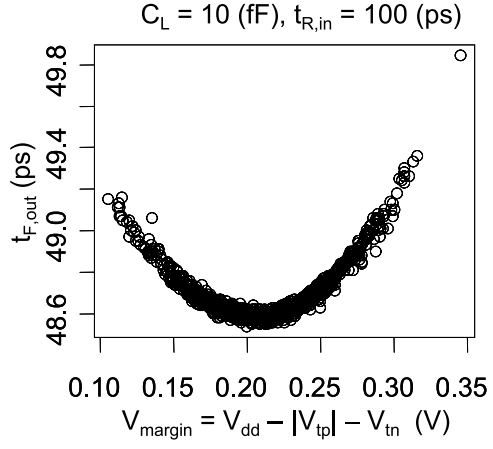

Fig. 7 Scatter plot of output transition-time and voltage margin (V_{margin}).

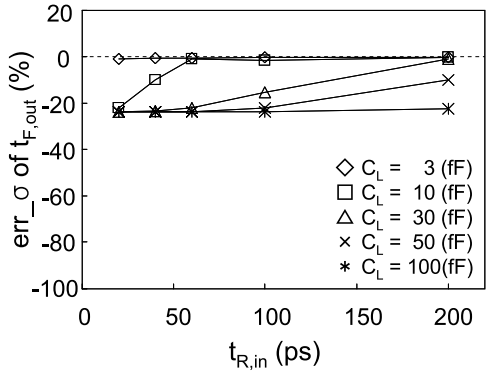

Fig. 9 err_σ (%) of the estimated output transition-time distribution by the quadratic relation of V_{margin}.

tive positions between threshold voltage distribution and $y0$. Figure 3(b) approximately corresponds to the worst condition where most of the threshold voltage distribution is projected around the minimal point and this is the reason why the error of the linear approximation exceeds 80% in Fig. 6(b).

Although analytical explanation of the cause of the quadratic relation has not been successful yet, we expect that it is originated from the resistance ratio (current ratio) of NMOS and PMOS transistors during output node transition.

4. Improving Estimation Accuracy of Output Transition-Time Variation

In this section, we propose an equation that improves estimation accuracy of the output transition-time variation better than by using either linear dependence on threshold voltage alone or quadratic dependence on V_{margin} only.

The linear dependence on NMOS threshold voltage and the quadratic dependence on the voltage margin are both related to the threshold voltage of transistors. They are caused by the two different trends that are complementally with each other. Thus, we propose the following expression to represent output transition-time tsl applicable for wide range of conditions.

$$tsl = (1 - r) \cdot tsl1 + r \cdot tsl2 \quad (5)$$

Here, $tsl1$ is the output transition-time distribution calculated by Eq. (1) based on the linear dependence of NMOS threshold voltage. In the second term, $tsl2$ is the output transition-time distribution calculated by Eq. (4) that is based on the quadratic relation of operating margin in voltage. r is the contribution ratio of the quadratic relation in the output transition-time distribution, which takes values in the range of [0, 1], and chosen to minimize the error of the equation.

We evaluated the computational accuracy of the output transition-time variation based on Eq. (5) by the following procedure.

i) Conduct SPICE Monte-Carlo simulations for all combinations of input transition-time and output load capacitance in Table 1.
ii) Approximate the parameters α, β in Eq. (1), a, $x0$, $y0$ in Eq. (4) and r in Eq. (5) through least square method from the results of i) for all combinations of input transition-time and output load capacitance.
iii) Compute output transition-time variations based on Eq. (5) using the approximated parameters in ii).
iv) Evaluate the accuracy of iii) against i) by using the variability error of Eq. (2) for all combinations of input transition-time and output load capacitance.

Figure 10 plots the approximated values of r in step ii) of the above procedure. The figure shows higher and lowers values of r according to lower and higher values of correlation coefficients in Fig. 2, respectively, which is interpreted as a complementary relationship between linear dependence on threshold voltage and quadratic dependence on V_{margin} as we expected.

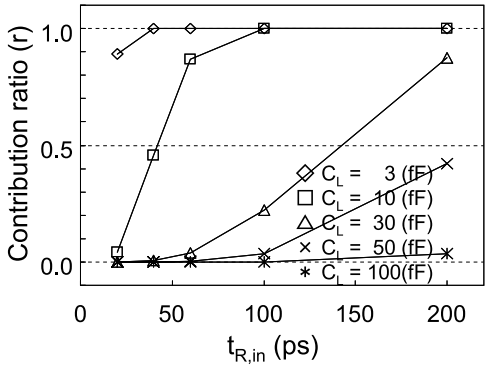

Fig. 10 The approximated values of contribution ratio of the quadratic relation (r) in Eq. (5).

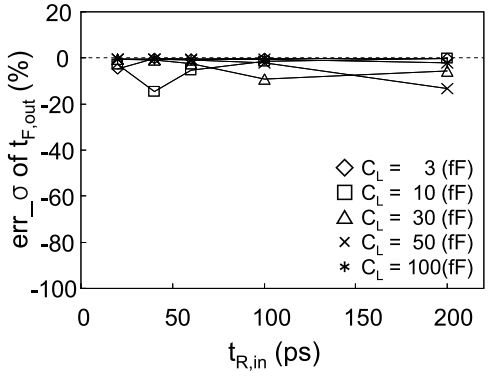

Fig. 11 err_σ (%) of the estimated output transition time distribution by our proposed method.

Table 2 Summary of err_σ (%) for the combinations of gate types and input pins. The 1st and 2nd rows show the result of conventional and our proposed method, respectively. The 3rd row shows the improvements of our proposed method over the conventional method.

		Inverter	NAND		NOR	
			A1	A2	A1	A2
Conv. (%)	Ave.	-12.83	-8.43	-6.85	-12.27	-16.47
	|Max|	88.89	75.91	61.58	41.67	92.66
	σ	19.96	17.48	15.18	14.98	23.82
Prop. (%)	Ave.	-2.79	-4.92	-2.61	-2.80	-5.54
	|Max|	14.52	23.59	13.80	15.16	36.62
	σ	4.05	6.67	3.24	4.36	10.45
Improv. (%)	Ave.	78.26	41.70	61.92	77.19	66.40
	|Max|	83.67	68.92	77.59	63.63	60.48
	σ	77.86	61.85	78.66	70.89	56.13

Figure 11 plots the variability error of our proposed method. In our approach, good accuracy within 15% to the SPICE Monte Carlo simulation has been observed in wide range of input transition-time and load capacitance combinations. Compared with the conventional approach having more than 80% error with the use of linear correlation characteristics only (Fig. 6(b)), improvement with our approach is significant. Note that a few percent of deteriorated points are observed in the figure (e.g. C_L = 10 (fF) and $t_{R,in}$ = 40 (ps)). The deterioration directly comes from the fact

that the objective function used for obtaining r is squared sum of errors at each measurement point, which is slightly different from the variance error in Eq. (2). The minimum of the squared error does not always correspond to the minimum of evaluation metrics, or variance error. Although the difference of objective functions worsens a few percents of our evaluation metric, our approach yields better accuracy in wide range of parameters.

Our example is about the falling output transition of CMOS inverter with 1.0 V supply voltage. However, through the same approach, we have also confirmed accuracy improvement for any combinations of rising/falling transitions, different gate types, and different supply voltages. Detailed experimental results of different gate types are shown in Appendix. Table 2 summarizes the results of CMOS inverter and other logic gates with average, maximum, and standard deviation of the variability error. Improvements over the conventional first-order sensitivity based approach are also shown. In the table, A1 and A2 identify signal input pins of the logic gates. Here, A2 drives power/ground side of series-connected transistors inside the gates, while A1 drives the other side. From the table, average and maximum errors are improved by 60% and 40%, respectively. Standard deviations of the variability error are also reduced more than 50%. Although a few deteriorated points are also observed in detailed results on Appendix section as could be found in inverter cases, our proposed approach can be generally improves estimation accuracy and applicable for wide range of parameters.

5. Conclusion

We analyzed output transition-time variation of logic gates and proposed an equation to improve its estimation accuracy under wide range of parameter variations. By applying a conventional first-order sensitivity-based approach only, the estimation error of CMOS inverter exceeds 80% in the cases of slow input transition-time and small output load combinations where the correlations of delay and output transition-time become low, even though it achieves good accuracy for higher correlation cases.

With our study on the output transition-time variation in the lower correlation cases, it has been shown that the output transition-time can be well approximated by quadratic relation of the voltage margin. Combining the conventional estimation for linear correlation cases and the estimation using quadratic relationship for lower correlation cases, we proposed an equation that can be generally used for different gate types and the combinations of input transition-time and output load capacitance. The estimation accuracy of the output transition-time variation can be significantly improved for wide range of parameter variations at least 60% of maximum and 40% of average by the proposed approach.

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Appendix

Tables A·1 through A·4 show the variability error of (a) our proposed method and (b) conventional first-order sensitivity-based approach for 2-input NAND gate and 2-input NOR gate. The circuit setup and experimental conditions are almost the same with Fig. 1 and Table 1 while assuming a perfect correlation among same types of transistors. The input pins (A1 or A2) that do not measure sig-

Table A·1 err_σ (%) of the estimated output transition-time distribution for A1 pin case of 2-input NAND.

$t_{R,in}$ (ps)

C_L (fF)	20	40	60	100	200
3	-10.80	-12.51	-23.59	-1.64	-0.15
10	-0.98	-4.14	-10.42	-11.98	-19.69
30	-0.44	-0.59	-0.91	-2.79	-12.19
50	-0.44	-0.58	-0.58	-0.90	-4.51
100	-0.44	-0.58	-0.58	-0.58	-0.89

(a) Proposed Method

$t_{R,in}$ (ps)

C_L (fF)	20	40	60	100	200
3	-3.95	-8.33	-22.96	-43.08	-27.61
10	-0.87	-1.39	-3.50	-8.44	-75.91
30	-0.44	-0.59	-0.82	-1.11	-5.00
50	-0.44	-0.58	-0.58	-0.81	-1.39
100	-0.44	-0.58	-0.58	-0.58	-0.80

(b) Conventional Method

Table A· 2 err_σ (%) of the estimated output transition-time distribution for A2 pin case of 2-input NAND.

C_L (fF) \ $t_{R,in}$ (ps)	20	40	60	100	200
3	-3.19	-13.80	-5.59	-4.03	-6.11
10	-0.70	-1.57	-3.89	-8.60	-2.36
30	-0.44	-0.59	-0.71	-1.26	-5.45
50	-0.44	-0.58	-0.58	-0.70	-1.87
100	-0.44	-0.44	-0.58	-0.58	-0.69

(a) Proposed Method

C_L (fF) \ $t_{R,in}$ (ps)	20	40	60	100	200
3	-1.93	-7.43	-61.58	-20.37	-16.40
10	-0.61	-1.01	-1.58	-3.53	-46.27
30	-0.44	-0.59	-0.71	-0.86	-1.90
50	-0.44	-0.58	-0.58	-0.70	-0.96
100	-0.44	-0.44	-0.58	-0.58	-0.69

(b) Conventional Method

Table A· 3 err_σ (%) of the estimated output transition-time distribution for A1 pin case of 2-input NOR.

C_L (fF) \ $t_{R,in}$ (ps)	20	40	60	100	200
3	-1.83	-0.21	-0.20	-0.19	-0.18
10	-2.55	-15.16	-6.90	-0.36	-0.13
30	-0.40	-0.94	-2.17	-8.44	-8.78
50	-0.40	-0.40	-0.75	-2.10	-14.15
100	-0.40	-0.40	-0.40	-0.49	-2.04

(a) Proposed Method

C_L (fF) \ $t_{R,in}$ (ps)	20	40	60	100	200
3	-33.39	-33.31	-28.89	-27.85	-27.40
10	-1.09	-7.81	-23.44	-41.67	-27.59
30	-0.40	-0.68	-0.98	-3.11	-37.29
50	-0.40	-0.40	-0.62	-0.96	-6.75
100	-0.40	-0.40	-0.40	-0.49	-0.94

(b) Conventional Method

Table A· 4 err_σ (%) of the estimated output transition-time distribution for A2 pin case of 2-input NOR.

C_L (fF) \ $t_{R,in}$ (ps)	20	40	60	100	200
3	-36.62	-4.66	-1.67	-0.82	-0.50
10	-1.32	-4.96	-36.14	-3.63	-0.59
30	-0.45	-0.72	-0.97	-5.24	-22.14
50	-0.42	-0.42	-0.64	-0.99	-12.28
100	-0.41	-0.41	-0.41	-0.50	-1.51

(a) Proposed Method

C_L (fF) \ $t_{R,in}$ (ps)	20	40	60	100	200
3	-92.66	-49.54	-37.94	-32.76	-30.26
10	-1.32	-4.96	-24.02	-52.88	-32.13
30	-0.45	-0.72	-0.97	-2.48	-38.25
50	-0.42	-0.42	-0.64	-0.93	-5.47
100	-0.41	-0.41	-0.41	-0.50	-0.92

(b) Conventional Method

nal delay are tied to logical high or low voltages so that the proper logic operations are enabled.

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