LETTER

An Experimental Study on Body-Biasing Layout Style Focusing on Area Efficiency and Speed Controllability

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SUMMARY Body-biasing is expected to be a common design technique, and then area efficient implementation in layout has been demanded. Body-biasing outside standard cells is one of possible layouts. However in this case body-bias controllability, especially when forward bias is applied, is a concern. To investigate the controllability, we fabricated and measured a ring oscillator in a 90 nm technology. Our measurement result and evaluation of area efficiency reveal that body-biased circuits can be implemented with area overhead of less than 1% yet with sufficient speed controllability.
key words: *body bias, layout*

1. Introduction

As technology advances, manufacturing variability has been becoming more and more significant. ITRS 2006 Update predicts that Vth variability and circuit performance fluctuation will continue to increase in the future. In addition, leakage power consumption will be soaring.

Recently, in order to address these problems, body-biasing technique has been studied. Forward body-bias is used to compensate manufacturing variability and reverse body-bias is used for reducing leakage power consumption [1], [2]. Therefore, body-bias technique will become more common and important, because both manufacturing variability and leakage power will become more severe.

When designing a body-biased circuit, standard cells tailored for body-biasing have been developed conventionally, and body contacts have been usually placed inside each cell for latch-up prevention. This layout has high body-bias controllability and latch-up prevention, however the area overhead is not negligible. As for latch-up prevention, its importance is becoming lower, because in advanced technologies with low supply voltage such as 1.0 V, latch-up is unlikely to happen [3], [4]. This enables us to use more area-efficient layout style in which body contacts are placed outside cells unlike the conventional layout style [3], [4].

A concern in such area-efficient layout style is that body-bias controllability may be degraded because longer distance between body contacts and MOS transistors involves large parasitic resistance, and even a small well current may change the potential of the MOS back-gate. When reverse body-bias is applied, well current is small and hence loss of controllability is expected to be small. However, it is not clear how much the controllability degrades when forward body-bias is applied to compensate speed variation.

In this work, we designed a test structure in a 90 nm process, and measured frequency of a ring oscillator with varied distances to body contacts. This measurement aims to reveal the relation between the controllability of body-bias including forward bias and the distance from body contacts to MOS transistors. We also examine area efficiency of the two layout styles. Based on measurement results and area efficiency evaluation, we finally discuss body-biasing layout style suitable for advanced technologies.

2. Layout Styles of Body-Biased Circuits

2.1 Conventional Within-Cell Biasing

A common layout style of body-biasing circuits, which is shown in Fig. 1(a), has two additional lines for supplying body-bias voltages to n-well and p-well. VDD and VSS are power and ground lines. VNW and VPW are body-bias lines for n-well and p-well respectively. We call this layout style "within-cell biasing style" in this paper, because the body-bias voltage is supplied inside each cell.

This layout style has two advantages. The first advantage is the high controllability of body-bias voltage, i.e. the VNW/VPW voltage can be accurately given to MOS transistors. The second advantage is high latch-up prevention. These advantages originate from sufficient body contacts placed close to MOS transistors. The parasitic resistance is small, and the well voltage can be fixed tightly. However, the area of circuits with within-cell biasing style is larger than that of conventional circuits without body-biasing because of added VNW and VPW lines.

Forward body-bias is more likely to trigger latch-up [3]. Thus, to prevent latch-up, within-cell biasing style has been used for body-biased circuits [5], [6].

2.2 Strap Biasing

As power supply voltage is lowered, latch-up becomes unlikely to happen [3]. Reference [4] reports that in a 90 nm-process circuit of which power supply voltage is 1 V or below, latch-up is not triggered even when body-bias voltage of −1 V to 1V is given. It is because power supply voltage is not sufficient for parasitic bipolar transistors of

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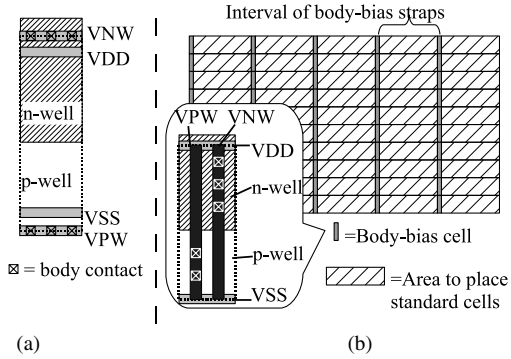

Fig. 1 Cell layout for body-biasing. (a) Within-cell biasing style, (b) Strap biasing style.

CMOS to turn on, and the gain of parasitic bipolar transistors in advanced processes is not sufficiently large to trigger/keep latch-up. From the analysis and measurement results, Ref. [4] pointed out a possibility that for low voltage circuits body contacts can be placed outside standard cells. A possible layout of this style is depicted in Fig. 1(b). A similar layout to Fig. 1(b) is suggested in [3]. The body-bias voltage is supplied through body-bias cells that are vertically placed as straps. We name this layout style "strap biasing style."

The main advantage of this style is that the circuit area is expected to be smaller than that of within-cell biasing style, which will be discussed in Sect. 4.1. A concern of strap biasing style is the controllability of body-bias voltage. The parasitic resistance of well between body contacts and MOS transistors is larger than that of within-cell biasing style. It may cause a rise/drop of body-bias voltage and make body-bias voltages of MOS transistors different instance by instance. When it happens, performance prediction becomes difficult, and then strap biasing can not be practically used. The body-bias controllability in strap biasing style is weakened as the strap interval becomes larger.

The important metrics in comparison of body-biasing styles are circuit area and controllability of body-bias. The controllability will be discussed in Sect. 3.2 and the circuit area is compared in Sect. 4.1.

3. Test Circuit Structure and Measurement Results

3.1 Test Circuit Structure

We designed a test structure (Fig. 2) to evaluate the controllability of body-bias in the strap biasing style. This circuit consists of 89-stage ring oscillators, where the leftmost one is used for the measurement and the others are dummies, and six pairs of body-bias voltage lines. The ring oscillators are constructed with 88 inverters and a two-input NAND. Each body-bias voltage line is connected to a micro pad. Lines #1 are adjacent to the leftmost ring oscillator, and the distance to lines #6 is 238.84 μm. We select one pair from the six pairs of body-bias voltage lines, and supply body-bias voltages.

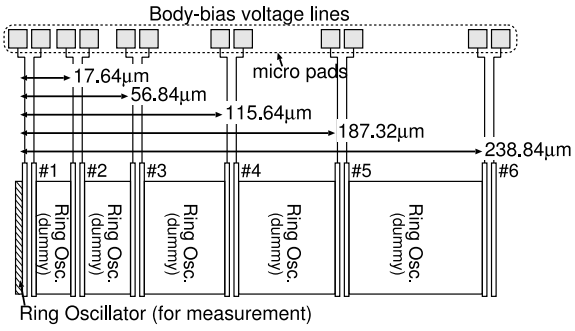

Fig. 2 Structure of test circuit.

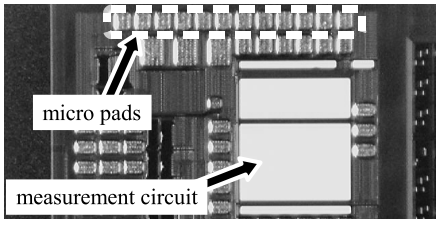

Fig. 3 Micrograph of fabricated test chip.

We measured the oscillation frequency of the leftmost ring oscillator through a 1024 divider, varying the body-bias supply position (pad), i.e. the distance from the body contacts to the ring oscillator as well as the body-bias voltage itself. The distance between the body contacts and transistors with pad pair #1 is the smallest, and it is almost equal to the distance of within-cell biasing style. Therefore, the controllability of #1 is expected to be the highest and correspond to that of within-cell biasing style. As the distance becomes longer, on the other hand, the controllability of body-bias may deteriorate. This deterioration can be observed as the oscillation frequency change. If the controllability is unchanged, the same oscillation frequency is measured. We define frequency variation by the following equation and use it as a metric of the speed controllability deterioration.

$$variation = \frac{\max(f_{\#1}, ..., f_{\#6}) - \min(f_{\#1}, ..., f_{\#6})}{f_{\#1}} \times 100$$

$f_{\#n}$ is oscillation frequency of line #n.

A test chip in Fig. 3 was fabricated in a 90 nm CMOS process with six metal layers and triple-well structure. N-well sheet resistance of the process is roughly 1k$\Omega/\square$. The size of the test circuit is 350 μm $\times$ 240 μm. We think 240 μm is wide enough because it costs only about 0.6% area overhead, which will be shown in Sect. 4.1.

3.2 Measurement Results

We measured the 1024-divided frequency of the ring oscillator with body-bias of -1 V to 1 V, changing pairs of body-bias lines from #1 to #6. We changed VPW and VNW simultaneously. The given power supply voltages are 1 V and 0.5 V. We measured at temperature of 25°C and 100°C. Figure 4 shows the measurement result at Vdd = 1 V and 25°C.

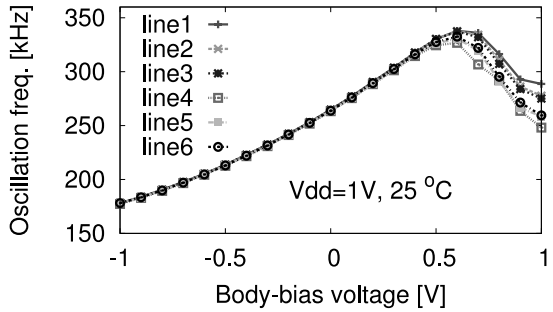

Fig. 4 Measured frequency of ring oscillator at Vdd = 1 V and 25°C.

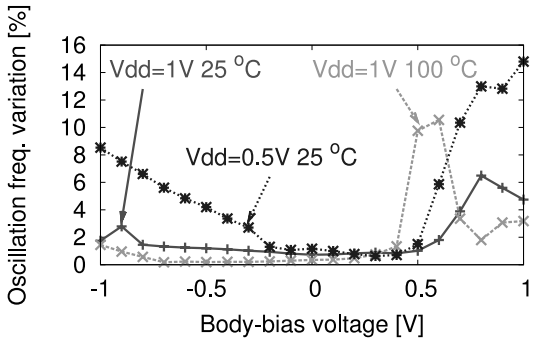

Fig. 5 Frequency variation among lines at {Vdd = 1 V, 25°C}, {Vdd = 1 V, 100°C} and {Vdd = 0.5 V, 25°C}.

The horizontal axis is the body-bias voltage and the vertical axis is the oscillation frequency. The distance between the leftmost ring oscillator and the body-biasing position has little effect on the ring oscillator frequency as long as the body-bias voltage is less than or equal to 0.5 V. Figure 5 shows that the frequency variation is less than 1.8% up to 0.5 V biasing at 25°C.

On the other hand, when the body-bias voltage becomes larger than 0.5 V, the measured oscillation frequency varies depending on the body-biasing position. But from a practical point of view, it is not a serious problem, because the oscillation frequency decreases when the body-bias voltage is beyond 0.6 V. The reason of this speed degradation is reported that increase in diffusion capacitance overwhelms increase in on-current [4]. In addition, applying such high forward body-bias voltage increases total current drastically as shown in Fig. 7.

When the temperature is 100°C, the oscillation frequency varies depending on positions of body contacts above 0.5V body-biasing (Fig. 5). On the other hand, Fig. 6 shows the circuit speed also begins to drop from 0.5 V body-bias. When the body-bias voltage is 0.4 V, the frequency variation is 0.97%. This means the controllability is sufficiently available under the effective range of body-bias voltage even when the body contacts are 240 μm distant.

Next, when the power supply voltage is 0.5V, high reverse body-bias degrades circuit controllability as well as high forward body-bias, which is shown in Fig. 5. On the other hand, such high reverse body-bias does not necessarily reduces power consumption [3]. Because, reverse body-bias decreases subthreshold leakage current, but it increases the junction tunneling leakage current of p-well and n-well shown in Fig. 8.

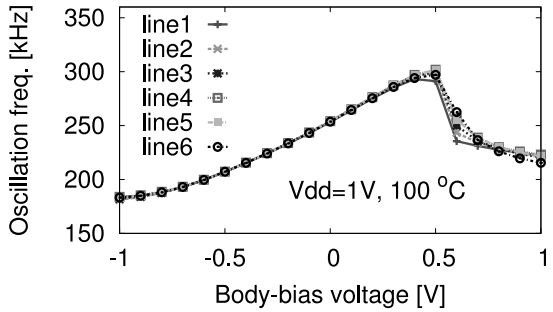

Fig. 6 Measured frequency of ring oscillator at Vdd = 1 V and 100°C.

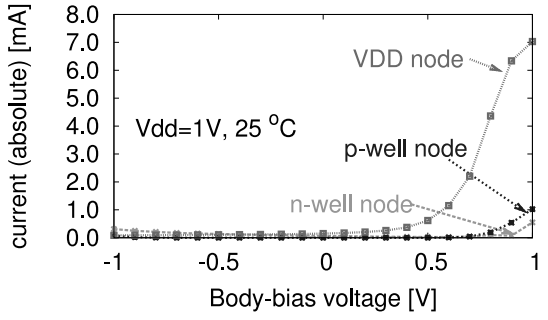

Fig. 7 Measured current at Vdd = 1 V and 25°C.

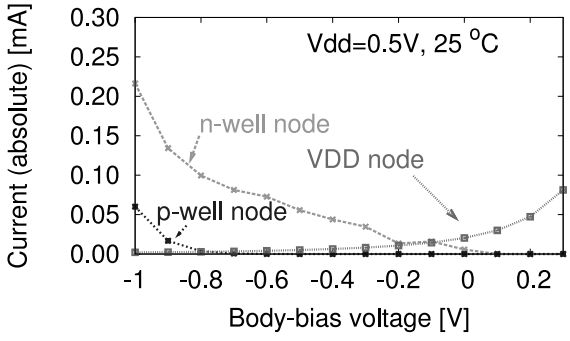

Fig. 8 Measured current at Vdd = 0.5 V and 25°C.

The speed controllability degrades at Vdd = 0.5 V even in the case of reverse body-biasing as shown in Fig. 5. When the supply voltage decreases close to the threshold voltage, the impact of the threshold voltage variation on the circuit speed becomes larger. To confirm this, we observed delay change of the inverter with SPICE simulation, shifting Vth of the inverter by 1mV. The delay change is 0.83% at Vdd = 0.5 V and 0.15% at Vdd = 1 V. Although the well-current is not so large compared with Fig. 7, the well-current could change the back-gate voltage of the ring oscillator. We think this is why the speed controllability degrades. This result implies using strap biasing style for reverse body-bias can be restricted in lower voltage operation. Nevertheless strap

biasing style works under beneficial body-bias range in this technology.

We here conclude that the strap body-biasing with 240 μm interval is effective under the beneficial range of body-bias in terms of speed improvement and power reduction, although the speed controllability degrades outside the beneficial range.

4. Discussion on Body-Biasing Layout Styles

4.1 Area Efficiency Evaluation

In this section, the area efficiency of two biasing styles is discussed. In within-cell biasing style, all cells are extended vertically to place two body-bias lines. In the case of standard cell library provided by the foundry, the cell height of within-cell biasing style is 1.22 times taller than that of fixed body-bias style. This results in 22% increase of circuit area.

In strap biasing style, strap interval is an important factor that determines area efficiency. We calculate area efficiency varying the strap interval with the following assumptions. We assumed a 1 mm-squared circuit and changed the strap interval from 10 μm to 240 μm. Here, 10 μm corresponds to the maximum cell width included in the standard cell library. When the interval is smaller than 10 μm, that cell is not placeable. We give a constraint that the area utilization of strap inserted circuit must be equal to or lower than the original circuit without straps, where the area utilization is defined as (total cell area)/(cell placeable area). This constraint is given to reserve the same space for clock buffer, routing and so on. We evaluated the area efficiency with the area utilization constraints of 0.50 and 0.85.

Figure 9 shows the relation between the body-bias strap interval and the circuit area. The vertical axis is the relative area normalized by the circuit area of fixed body-bias circuit. Figure 9 demonstrates that strap biasing style is more area-efficient than within-cell biasing style for any strap interval. The area efficiency improves as the strap interval increases. The curves of 0.50 and 0.85 utilization constraints are very close to each other, which means that the area efficiency is independent of the utilization ratio.

4.2 Wire Length Evaluation

Next, we evaluate the increase in wire length. We actually designed layouts of body-biased and fixed body-biased circuits. The circuit used for the experiment is a 64-bit multiplier whose cell count is 49 k. The layout size is roughly 500 μm $\times$ 500 μm in fixed body-bias style. We selected two strap intervals of 10 μm and 240 μm. The total interconnect length and circuit area are listed in Table 1. The wire length and circuit area are normalized by those of fixed body-biasing respectively. In the case of within-cell biasing and strap biasing with 10 μm interval, the total wire length increases by 7–8%. On the other hand, in the case of strap biasing with 240 μm interval, the wire length increase is within 1%, and hence the impact on performance is expected to be negligible.

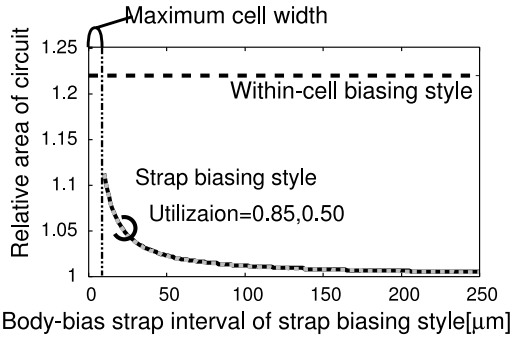

Fig. 9 Area efficiency of strap biasing style with varied strap intervals (curved lines). Horizontal dashed line corresponds to within-cell biasing style.

Table 1 Total wire length and circuit area.

Biasing layout style	Wire length (*)	Circuit area (*)
Fixed body-bias	1	1
Within-cell biasing	1.077	1.222
Strap biasing (10 μm interval)	1.066	1.110
Strap biasing (240 μm interval)	1.010	1.007

* relative

As shown in Sect. 3, the strap body-biasing with 240 μm interval is good enough under the beneficial body-bias range. The area increase and the wire length increase is less than 1% at that interval. The interval wider than 240 μm might be still possible in terms of speed controllability, however it would provide little improvement in area efficiency.

5. Conclusion

In this paper, we discussed body-biasing layout styles focusing on speed controllability and area efficiency. To investigate the speed controllability, we designed a test structure in a 90 nm technology. From the measurement results, the distance of 240 μm is acceptable even when forward body-bias is applied. We then evaluated area efficiency of strap biasing style and showed that area increase was less than 1% when the strap interval was 240 μm. We also confirmed that the impact on wire length was limited within 1%. We thus conclude that strap biasing style with large strap interval is efficient both in area efficiency and speed controllability.

Acknowledgment

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