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Analytical Eye-Diagram Model for On-Chip Distortionless Transmission Lines and Its Application to Design Space Exploration

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SUMMARY This paper proposes a closed-form eye-diagram model for on-chip distortionless transmission lines with intentionally inserted shunt conductance. We derive expressions of eye-opening both in voltage and time, by assuming a piece-wise linear waveform model. The model is experimentally verified with various length, shunt conductance and resistive termination. We also apply the proposed model to design space exploration, and demonstrate that the proposed model helps estimate the optimal shunt conductance and resistive termination according to required signaling length and throughput.

key words: *eye-diagram, on-chip transmission line, waveform distortion, resistive termination, shunt conductance*

1. Introduction

On-chip interconnection has become one of the problems preventing performance enhancement in advanced technologies. As one of promising solutions, high-speed signaling over on-chip transmission lines has been studied both in circuit and EDA communities [1]–[3]. In this scheme, maximum throughput of on-chip transmission lines is a primary concern. Reference [4] reports that, in the current technology, the interconnect throughput is superior to transistor performance, and the signaling throughput is predicted to improve thanks to transistor performance enhancement in the future.

For further improvement of signaling throughput, intersymbol interference (ISI) is a critical obstacle. Due to frequency dependence of propagation characteristics, the pulse distorts. Pre-emphasis at a driver and equalization at a receiver are effective for suppressing ISI and widely used in chip-to-chip communication [5]. Recently, on-chip transmission line with less distortion has been also studied [6]–[9]. References [6], [7] demonstrate that nonlinear transmission lines with active variable capacitance enable signaling with less dispersion and loss.

References [8], [9] proposed on-chip transmission lines with shunt resistance intentionally inserted for suppressing distortion. Thanks to S_iO_2 characteristics, the conductance of on-chip transmission lines can be kept negligibly small by isolating the lines from S_i substrate. According to transmission line theory, when a condition $RC = GL$ holds, attenuation and phase velocity become constant over all frequency range, and waveform distortion disappears. References [8], [9] intentionally insert shunt conductance to satisfy $RC = GL$, assuming shunt conductance is implemented by poly silicon. ISI reduction by shunt resistance is clearly demonstrated [8], [9], though the distortionless condition can not be satisfied in all frequency, because R and L are frequency dependent due to skin and proximity effects. In reality, as the shunt conductance approaches to to $G = RC/L$, the frequency dependence of attenuation and phase velocity are suppressed gradually. On the other hand, the inserted shunt conductance increases the attenuation, and hence the suppression of distortion and the signal magnitude are in a trade-off relationship. When ISI is severe, shunt conductance improves the eye-diagram. On the other hand, when ISI and signal magnitude are small, shunt conductance should not be inserted. Therefore, optimal shunt resistance value to maximize opening in eye-diagram depends on interconnect length and signaling throughput. In addition, resistive termination is widely used to reduce ISI for high-speed signaling. However, it is not clear how to determine termination resistance for shunt-inserted transmission lines.

This paper proposes an analytic eye-diagram model for shunt-inserted distortionless transmission lines. The proposed model can derive the optimal shunt resistance and termination resistance without time-consuming circuit simulation. We extend the model of voltage eye-opening [10]–[12] for the shunt-inserted transmission lines. We also derive a closed-form expression of eye-opening in time. We demonstrate that the optimal shunt resistance and termination resistance change drastically depending on interconnect length and signaling throughput. Our analytical model is useful for rough performance estimation and design space exploration early in a design stage.

This paper is organized as follows. Section 2 explains signal propagation on transmission lines and ISI reduction thanks to shunt conductance and resistive termination. Section 3 explains the proposed analytic model, and verifies the estimation accuracy. Section 4 shows a trade-off analysis in shunt and termination resistances by using the proposed model. Section 5 concludes the paper.

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2. Signal Propagation on Shunt-Inserted Transmission Lines with Resistive Termination

We first review signal propagation on shunt-inserted transmission lines with resistive termination.

The circuit model of terminated transmission-lines is shown in Fig. 1. The resistance, inductance, conductance and capacitance per unit length are R, L, G and C respectively. The impedance Z_0 is the characteristic impedance of transmission-line. At the receiver side, the interconnect is terminated by a resister and the resistance value is R_t. At the driver side, we assume that the driver of the interconnect achieves impedance matching. In other words, the output impedance of the driver is equal to the characteristic impedance Z_0. The amplitude of the voltage source is V_{dd}. Differential signaling with bridge termination can be discussed similarly [10], [11], and hence we here suppose a single-end circuit model.

On transmission lines, the voltage at any point along the line of length z is expressed as

$$V(z) = V_{near}e^{-\gamma z} = V_{near}e^{-(\alpha+j\beta)z}, \quad (1)$$

where V_{near}, which is the amplitude of the pulse injected to the interconnect, is expressed as $V_{near} = V_{dd}/2$, because the driver output impedance is equal to the characteristic impedance Z_0 in Fig. 1. γ is the propagation constant and represented as

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta. \quad (2)$$

α, which is the real part of γ, is the attenuation constant. β is the imaginary part of γ and the phase constant.

To reduce ISI and improve signaling throughput, resistive termination is widely used. When R_t is equal to Z_0, no reflection occurs at the far-end, and degradation of signal integrity due to multiple reflection is eliminated. On the other hand, the voltage magnitude becomes $0.5V_{dd}$ although the voltage reaches to V_{dd} when the far-end is not terminated. In the case of on-chip transmission lines, the attenuation is significant and multiple reflection has little effect on signal integrity. For example in the structure shown in Fig. 2, which will be used for experimental model validation in Sect. 3.4, α is 2.73×10^2 at 10 GHz, and the signal is attenuated by 67% for a 4 mm-long traversal. Thus, the optimal termination, which is not necessarily Z_0, was studied in Refs. [11], [12].

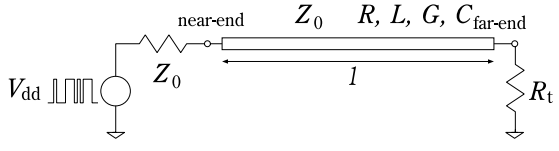


Fig. 1 Circuit model of a transmission-line with resistive termination.

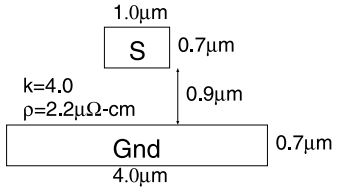


Fig. 2 Wire cross-section.

Another approach to reduce ISI has been proposed in Refs. [8], [9]. To reduce frequency dependency of the propagation constant γ, shunt conductance is intentionally inserted to satisfy distortionless condition of $RL = GC$. When $G = RL/C$, the attenuation constant α and the phase velocity ω/β become frequency independent and are expressed as $R/\sqrt{L/C}$ and $1/\sqrt{LC}$. Similarly, the characteristic impedance Z_0 becomes frequency independent and is $\sqrt{L/C}$. As long as the frequency dependency of R, L, G and C is not significant, a distortionless transmission line can be realized.

Here let us show an example that shunt conductance and resistive termination improve the eye-diagram. The experimental conditions are the same with Sects. 3.4 and 4. 40 Gbps signal transmission on a 6 mm Cu wire is assumed. Figure 3 shows eye-diagrams. We can see that shunt insertion of $G = 3.34$S improves the eye-diagram (Figs. 3(b), (c)) and resistive termination of $R_t = 114\,\Omega$ reduces the jitter (Figs. 3(a), (c)), although both reduces the voltage magnitude.

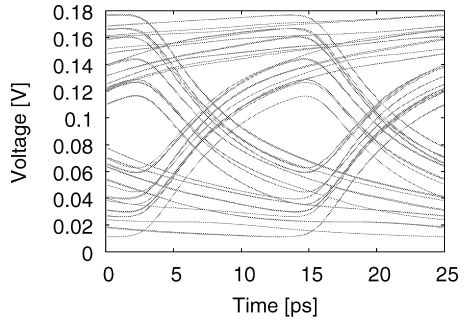
The intentional shunt G insertion obviously increases the attenuation, and reduces the signal magnitude. The shunt conductance has a trade-off between ISI reduction and magnitude degradation. Therefore, derivation of optimal shunt conductance and resistive termination considering required throughput and signaling length is necessary. The following section discusses analytical estimation of eye-diagram, and describes how to estimate eye-opening in voltage and time indicated in Fig. 3(c).

3. Analytical Eye-Diagram Model

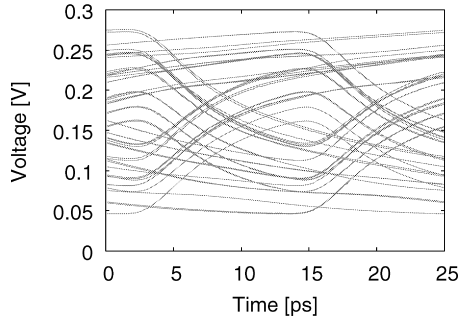
This section describes an analytical eye-diagram model for shunt-inserted transmission lines, and experimentally validates the model.

3.1 Piecewise-Linear Waveform Model

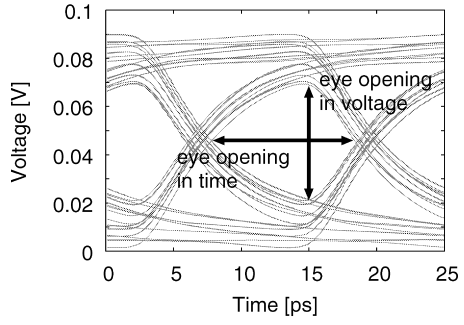
We here introduce a piecewise-linear (PWL) waveform model proposed in Refs. [10]–[12]. We model the waveform at the receiver side of transmission-lines by the PWL waveform model shown in Fig. 4. Figure 4 is the eye-diagram by two isolated pulse ($0\cdots010\cdots0$ and $1\cdots101\cdots1$). When noise is small, these isolated pulses determine the eye-opening in voltage. Time t_r is the transition time of input pulse injected by the driver, and we assume that the same transition time appears at the receiver as shown in Fig. 4. Period T is the minimum width of input pulse. Voltage V_r is the rise voltage that is determined from the attenuation and the termination of the interconnect. The voltage V_T is the voltage at the time T. The voltage V_T decides the maximum eye-opening voltage. The voltage V_{max} is the voltage level



(a) $G = 3.34$ **S** and $R_t = 10\text{k}\Omega$



(b) $G = 0.1$ **mS** and $R_t = 114\Omega$



(c) $G = 3.34$ **S** and $R_t = 114\Omega$

Fig. 3 An example of eye-diagrams w/ and w/o shunt conductance and resistive termination.

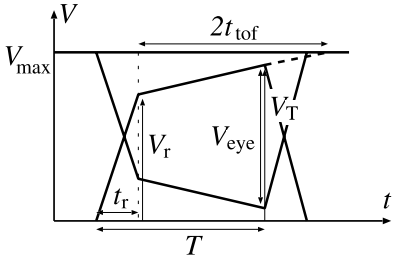


Fig. 4 PWL waveform model.

when the continuous "1" is input to the interconnect. The voltage $V_{\max}$ is determined by the resistance of the terminator, the resistance and conductance of the interconnect and the output resistance of the driver. The time t_{tof} is the signal time-of-flight, i.e. it is the time needed for one-way wave traversal and is determined by the interconnect length and the velocity of electromagnetic wave. We approximately estimate t_{tof} as $l/\sqrt{LC}$ in this paper. Reference [11] analytically points out that when the driver achieves impedance matching for a frequency-independent transmission line, the voltage at the receiver side reaches $V_{\max}$ at the time when $2t_{\text{tof}}$ passed after the rising. Reference [12] experimentally validates that this characteristic reasonably holds even for frequency-dependent transmission lines. By using this characteristic, we can derive the voltage V_{T}.

From the PWL waveform model in Fig. 4, the maximum eye-opening voltage V_{eye} is expressed as

$$V_{\text{eye}} = \begin{cases} \max\{V_{\max} - 2\,(V_{\max} - V_{\text{T}}),\, 0\} & (T - t_{\text{r}} < 2t_{\text{tof}}) \\ V_{\max} & (T - t_{\text{r}} > 2t_{\text{tof}}) \end{cases}, \tag{3}$$

where $\max(A, B)$ function returns A when $A \geq B$ and B in the other case. The resistive termination changes V_{T} and $V_{\max}$. The shunt conductance also varies V_{T} and $V_{\max}$. Therefore, designers can tune the eye-opening by resistive termination and shunt resistance.

3.2 Derivation of Eye-Opening in Voltage

The amplitude of the pulse injected by an impedance-matched driver is $V_{\text{near}} = V_{\text{dd}}/2$, and the pulse attenuates as propagating on the lossy transmission-line. The amplitude of the attenuated pulse at the receiver side is expressed as

$$V_{\text{far}} = V_{\text{near}} \exp(-\alpha l) = n\mathbf{V}_{\text{dd}}/2, \tag{4}$$

where the parameter α is the attenuation constant of the interconnect and the parameter n is the attenuation parameter defined as $n = \exp(-\alpha l)$. As the attenuation becomes weaker, the parameter n becomes larger. If the line is lossless, the parameter n is equal to 1. From Eq. (2), α is expressed as follows.

$$\alpha = \text{Re}\left[\sqrt{(R + j\omega L)(G + j\omega C)}\right], \tag{5}$$

$$= \sqrt{\frac{-\omega^2 CL + \omega C\sqrt{\omega^2 L^2 + R^2}}{2}}. \tag{6}$$

The reflection coefficient Γ at the receiver side is expressed as $(R_{\text{t}} - Z_0)/(R_{\text{t}} + Z_0)$. Therefore, the rise voltage V_{r} is calculated by

$$V_{\text{r}} = V_{\text{far}} \times (1 + \Gamma) = \frac{n\mathbf{V}_{\text{dd}}}{2}\frac{2Z_{\text{n}}}{Z_{\text{n}} + 1}, \tag{7}$$

where the parameter Z_{n} is the normalized impedance defined as $Z_{\text{n}} = R_{\text{t}}/Z_0$. $Z_{\text{n}} = 0$ means short-circuit termination, $Z_{\text{n}} = 1$ means matched termination and $Z_{\text{n}} = \infty$ means open-ended.

The maximum voltage $V_{\max}$ is determined by DC characteristics of the transmission line, and hence it is expressed as R, G, R_{t} and l. $V_{\max}$ is derived with the RG ladder circuit

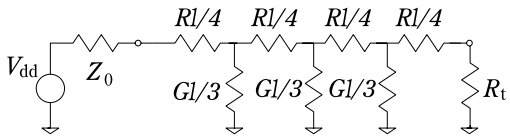


Fig. 5 Circuit model for $V_{\max}$ derivation.

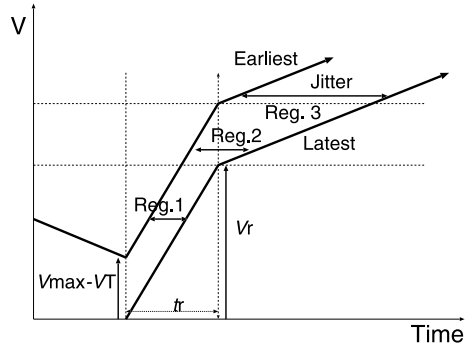


Fig. 6 Jitter model.

shown in Fig. 5. Even when the number of shunt conductance is larger than three, $V_{\max}$ scarcely changes, and hence we calculate $V_{\max}$ with Fig. 5. In this case, $V_{\max}$ is expressed as follows.

$$V_{\max} = \frac{R_t \mathbf{V}_{dd}}{(Z_0 + Rl/4)(1 + \frac{R_t + Rl/4}{Gl/3} + A + B) + B \cdot Gl/3}, \quad (8)$$

$$A = \frac{1}{Gl/3}\left(\frac{Rl}{2} + \frac{Rl}{4}\left(\frac{R_t + Rl/4}{Gl/3}\right) + R_t\right), \quad (9)$$

$$B = \frac{1}{Gl/3}\left(\frac{Rl}{4}\left(1 + \frac{R_t + Rl/4}{Gl/3} + A\right) + A \cdot Gl/3\right). \quad (10)$$

The voltage V_T is expressed in the PWL waveform model of Fig. 4 as

$$V_T = V_r + (V_{\max} - V_r)\frac{T - t_r}{2t_{tof}}. \quad (11)$$

We thus calculate V_{eye} of Eq. (3) analytically.

3.3 Derivation of Eye-Opening in Time

We next derive a closed-form expression for eye-opening in time. Without DC bias, the eye-opening in time becomes maximum when the voltage is $V_{\max}/2$. As shown in Fig. 6, the latest rise transition starts from $V = 0$. On the other hand, the earliest transition begins at $V = V_{\max} - V_T$. The jitter is the $V_{\max}/2$ crossing time difference between the earliest and latest transitions. As indicated in Fig. 6, there are three regions for calculating jitter: Region1 ($V_r > V_{\max}/2$), Region2 ($V_r < V_{max}/2$ & $V_{\max} - V_T + V_r > V_{\max}/2$), and Region3 ($V_r < V_{\max}/2$ & $V_{\max} - V_T + V_r < V_{\max}/2$).

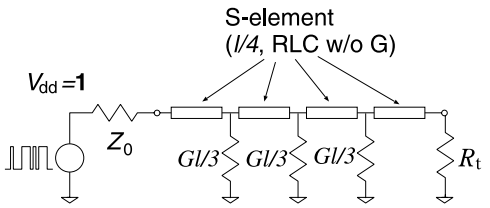


Fig. 7 Setup for model verification.

$$Jitter = \begin{cases} \frac{V_{\max} - V_T}{V_r} t_r \\ \quad \left(V_r > \frac{V_{\max}}{2}\right), \\ \frac{V_{\max} - 2V_r}{V_{\max} - V_r} t_{tof} + \frac{V_{\max} - 2V_T + 2V_r}{2V_r} t_r \\ \quad \left(V_r < \frac{V_{\max}}{2} \ \& \ V_{\max} - V_T + V_r > \frac{V_{\max}}{2}\right), \\ \frac{V_{\max} - V_T}{V_{\max} - V_r} 2t_{tof} \\ \quad \left(V_r < \frac{V_{\max}}{2} \& V_{\max} - V_T + V_r < \frac{V_{\max}}{2}\right). \end{cases} \quad (12)$$

The eye-opening in time is $T - Jitter$.

3.4 Model Verification

We verify the appropriateness of the proposed analytic model. We here use an on-chip microstrip transmission-line shown in Fig. 2 for experiments. The relative permittivity of insulator is 4.0, and the metal conductivity is $2.2\,\mu\Omega$·cm. The resistance, inductance and capacitance are computed by a commercial 2-D field solver from DC to 10 THz. At DC, they are $3.54 \times 10^4\,\Omega$/m, 4.35×10^{-7}H/m and 1.32×10^{-10} F/m. $\sqrt{L/C}$ is $57.5\,\Omega$ and $1/\sqrt{LC}$ is 1.32×10^8 m/s at DC. When we compute eye-opening in voltage and time with the derived expressions, we use RLC values at the frequency of $\frac{1}{2T}$. Figure 7 shows the circuit setup for simulation. We here model the RLC transmission line whose length is $l/4$ as an S-element implemented in HSPICE, where s-parameters are described in S-element. The simulation considers the frequency dependence of interconnect characteristics. Three shunt conductance of $Gl/3$ are inserted between the successive S-elements. We confirmed that the simulation results were almost unchanged even if the number of wire and shunt segments increased. PRBS pulses are given to the driver, and measure the eye-diagram at the far-end. t_r is set to $0.1T$, and V_{dd} is assumed to be 1.0 V.

We first verify the accuracy of eye-opening in voltage. Figure 8 shows the eye-opening vs. transmission speed. The interconnect length is 6 mm and R_t is $100\,\Omega$. Three lines correspond to the estimation results of the proposed model, and the conductance values are different. The dots are the circuit simulation results. The conductance value changes the eye-opening, and the proposed model estimates it well. As the transmission speed becomes faster, the eye-opening decreases. This tendency is also estimated by the model.

We next vary the shunt conductance and the termination resistance in 6 mm-long 20 Gbps transmission. In

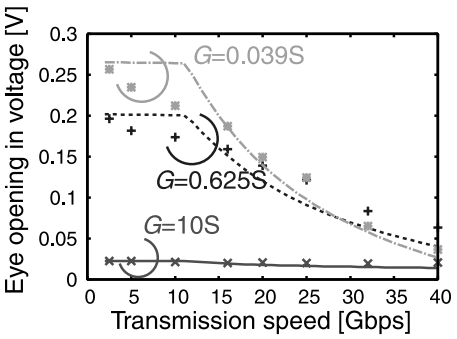


Fig. 8 Eye-opening in voltage vs. transmission speed (6 mm, R_t = 100 Ω).

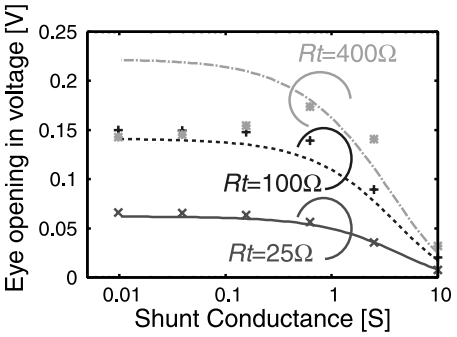


Fig. 9 Eye-opening in voltage vs. shunt conductance (6 mm, 20 Gbps).

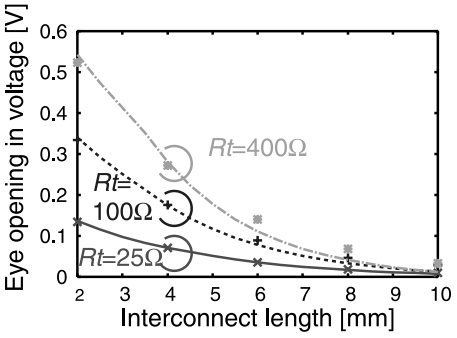


Fig. 10 Eye-opening in voltage vs. interconnect length (G = 2.5 S, 20 Gbps).

this configuration, larger termination resistance and smaller shunt conductance enlarge eye-opening (Fig. 9). In the case of R_t = 400 Ω with small shunt conductance, the estimation error is large. Even if impedance mismatch at the far-end causes a large reflection, multiple-reflection would not arise because of impedance matching at the driver side. However, in reality, perfect impedance matching is impossible because of frequency dependence of characteristic impedance. Thus, a certain amount of estimation error is introduced.

Figure 10 shows the eye-opening in voltage vs. interconnect length. The shunt conductance is 2.5 S, and the transmission speed is 20 Gbps. We can see that the decreasing tendency of eye-opening is well estimated by the proposed model.

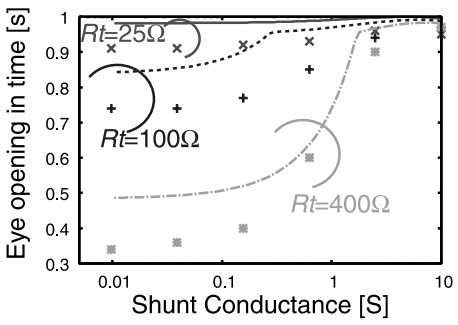


Fig. 11 Eye opening in time vs. shunt conductance (6 mm, 20 Gbps).

We finally verify the appropriateness of the eye-opening in time. Figure 11 shows the eye-opening in time estimated by the proposed model and circuit simulation. The vertical axis is the eye-opening in time normalized by the cycle time (1-$Jitter/T$). As the shunt conductance becomes small, the eye-opening decreases. This means the shunt conductance reduces ISI, whereas it decreases eye-height as shown in Fig. 9. The superiority of less ISI and the inferiority of eye-height decrease in shunt-inserted transmission lines are well modeled.

We thus conclude that the proposed model is useful to roughly explore the design space of on-chip transmission lines in terms of shunt conductance, termination resistance, transmission speed and so on. After we find a good design point from the explored design space, we perform detailed tuning of design parameters around the point with accurate yet time-consuming simulators, which can save design time and/or extend the design space we can explore.

4. Design Space Exploration

This section discusses shunt conductance and termination resistance that maximize signaling performance. When the signaling speed is not high and ISI is small, insertion of shunt conductance only reduces the signal magnitude, and it is not desirable. On the other hand, when bit-rate is high, ISI degrades signal integrity, and in this case, shunt insertion is effective. We here evaluate the trade-off of signaling performance with respect to shunt conductance and termination resistance, and reveal that the proposed model is useful for the design space exploration early in the design stage.

Suppose 6 mm-long 10 Gbps signal transmission with the microstrip structure in Fig. 2. We here evaluate the product of the eye-opening in voltage and that in time normalized by the cycle time for simplicity, expecting that the product is related to the opening area of the eye-diagram. The result is shown in Fig. 12. The contour lines of the product of eye-openings in voltage and time are drawn on the bottom. In this configuration, high termination resistance and small shunt conductance are expected to enlarge the eye-area opening. On the other hand, when the signaling speed goes up to 40 Gbps, the optimal values become much different (Fig. 13). Shunt conductance of 3.34 S and termination resistance of 114 Ω maximize the product The optimal

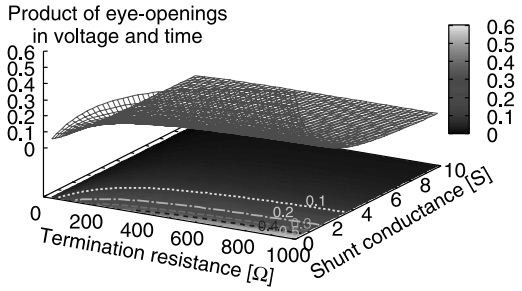


Fig. 12 Product of eye-openings in voltage and time with various termination resistance and shunt conductance (6 mm, 10 Gbps).

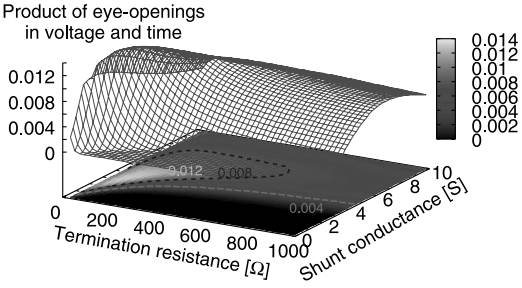


Fig. 13 Product of eye-openings in voltage and time with various termination resistance and shunt conductance (6 mm, 40 Gbps).

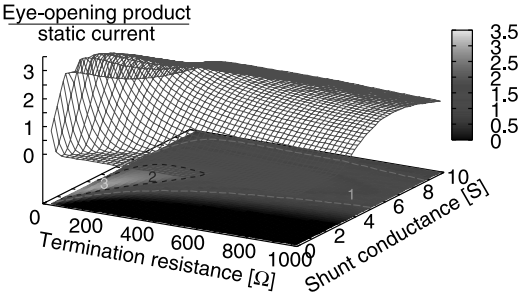


Fig. 14 Eye-opening product/static current (6 mm, 40 Gbps).

values depend on signaling speed and interconnect length. The proposed model can show the performance trade-off quickly, and hence it is helpful early in the design stage.

We finally show another performance analysis. Static power consumption is an important performance metric, and hence it is considered in this experiment. The vertical axis of Fig. 14 is the eye-opening product divided by static current. Here, the static current is the DC current of the voltage source in Fig. 5, and its analytic expression is easily derived. The optimal values of R_t and G are 81.5 Ω and 2.97 S. We can easily analyze various performance trade-offs.

5. Conclusion

This paper proposed a closed-form expression of eye-opening for shunt-inserted on-chip transmission lines. The eye-openings in voltage and time are derived analytically and experimentally verified in accuracy. We demonstrated trade-off analysis with the proposed model in terms of shunt conductance and termination resistance. The optimal values are dependent on signaling configuration, and the design space exploration early in the design stage is enabled by the proposed model.

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References

[1] M. Hashimoto, A. Tsuchiya, and H. Onodera, "On-chip global signaling by wave pipelining," Proc. EPEP, pp.311–314, 2004.
[2] H. Ito, J. Inoue, S. Gomi, H. Sugita, K. Okada, and K. Masu, "On-chip transmission line for long global interconnects," Proc. IEDM, pp.677–680, 2004.
[3] M.P. Flynn and J.J. Kang, "Global signaling over lossy transmission lines," Proc. ICCAD, pp.985–992, 2005.
[4] M. Hashimoto, A. Tsuchiya, A. Shinmyo, and H. Onodera, "Performance prediction of on-chip high-throughput global signaling," Proc. EPEP, pp.79–82, 2005.
[5] S.C. Thierauf, High-Speed Circuit Board Signal Integrity, Artech House, 2004.
[6] E. Afshari and A. Hajimiri, "Nonlinear transmission lines for pulse shaping in silicon," IEEE J. Solid-State Circuits, vol.40, no.3, pp.744–752, 2005.
[7] J. Kim, W. Ni, and E.C. Kan, "A novel global interconnect method using nonlinear transmission lines," Proc. CICC, pp.617–620, 2005.
[8] H. Chen, R. Shi, C.K. Cheng, and D.M. Harris, "Surfliner: A distortionless electrical signaling scheme for speed of light on-chip communications," Proc. ICCD, pp.497–502, 2005.
[9] H. Zhu, R. Shi, C.K. Cheng, and H. Chen, "Approaching speed-of-light distortionless communication for on-chip interconnect," Proc. ASP-DAC, pp.684–689, 2007.
[10] A. Tsuchiya, M. Hashimoto, and H. Onodera, "Performance limitation of on-chip global interconnects for high-speed signaling," IEICE Trans. Fundamentals, vol.E88-A, no.4, pp.885–891, April 2005.
[11] A. Tsuchiya, A Study on Modeling and Design Methodology for High-Performance On-Chip Interconnection, Ph.D. Dissertation, Kyoto University, 2005.
[12] A. Tsuchiya, M. Hashimoto, and H. Onodera, "Optimal termination of on-chip transmission-lines for high-speed signaling," IEICE Trans. Electron., vol.E90-C, no.6, pp.1267–1273, June 2007.

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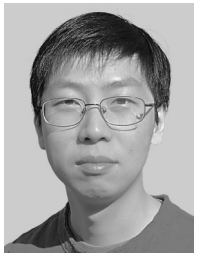

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