Measurement of Supply Noise Suppression by Substrate and Deep N-well in 90nm Process

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Abstract—**This paper measures and compares power supply and ground noises in a triple-well structure and a twin-well stricture. The measurement results of power supply and ground waveforms in a 90nm CMOS process reveal that the power noise reduction thanks to the increased junction capacitance associated with the triple-well structure overwhelms the ground noise suppression due to the resistive network of p-substrate in the twin-well structure. These noise suppression effects are well correlated with the simulation that uses on-chip RC power distribution model with package inductance, chip-level p-substrate resistive mesh and distributed well junction capacitances.**

Fig. 1.   Cross-section and parasitic elements in twin-well structure.

I. INTRODUCTION

Power supply noise is becoming a serious issue in recent processes. Design of stable power supply network is highly required, and hence accurate estimation of power supply noise is crucial for successful physical design. Power distribution network is often analyzed with current consumption of a circuit, resistance and inductance of wire and package, and capacitance [1], [2]. In addition, in a conventional design with a twin-well structure, V_{ss} is connected to p-substrate to supply backgate voltage. The resistive network of the p-substrate makes V_{ss} voltage stable, which has been discussed with simulation [3], [4] and measurement [5].

In recent processes, a triple-well structure, which involves additional fabrication cost, is often adopted for body biasing in high performance and low power design [6] and for substrate noise reduction in mixed SoC design [7]. V_{ss} is isolated from the p-substrate by deep n-well in the triple-well structure, and the supply noise suppression thanks to the resistive network of the p-substrate is immunized. On the other hand, PN junction capacitance involved with the deep n-well may work as intrinsic decoupling capacitance and reduce power supply noise. Although substrate noise reduction in the triple-well structure has been actively discussed [7], it has not been reported with a solid measurement how the triple-well structure affects power supply and ground noises, i.e., whether the triple-well structure increases or decreases power supply noise as far as the authors know.

This paper measures V_{dd} and V_{ss} noise waveforms on a test chip fabricated in a 90nm CMOS process, and clearly reveals the impact of substrate and deep n-well on power supply and ground noises comparing the twin-well and triple-well structures. In the twin-well structure, thanks to the resistive network of p-substrate, V_{ss} noise is somewhat smaller than that in the triple-well structure. On the other hand, V_{dd} noise in the triple-well structure is much smaller than that in the
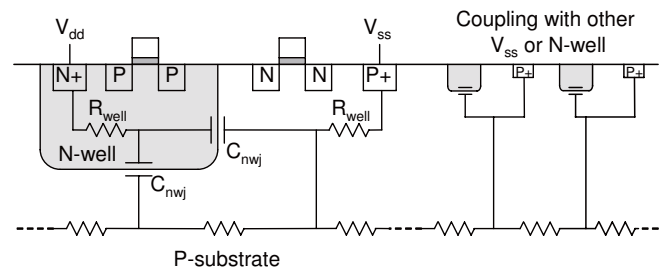
twin-well structure. The measurement results point out that the triple-well structure reduces power supply noise rather than increases supply noise. We also show simulation results of V_{dd} and V_{ss} noises both in the twin-well and triple-well structures, and demonstrate that the simulation results with a chip-level substrate and junction capacitance model are well correlated with the measurement results.

The remaining of this paper is organized as follows. Section II describes the twin-well and triple-well structures and their impact on power supply noise. Section III explains a measurement circuit used for evaluation. Section IV shows measured noise waveforms and discusses noise suppression effect of substrate and well junction capacitance. The measurement results are supported with simulation results in Section V. Section VI concludes this paper.

II. TWIN-WELL AND TRIPLE-WELL STRUCTURES AND POWER SUPPLY NOISE

Figure 1 depicts a cross-section of a twin-well structure with intrinsic parasitic elements. V_{dd} and V_{ss} are usually connected to n-well and p-substrate respectively in cell-based design to provide backgate voltage to transistors. The substrate is modeled as a resistive network. PN junction between the n-well and the p-substrate is modeled as capacitance (C_{nwj}), and works as decoupling capacitance. Thanks to the resistive substrate network, the impedance of V_{ss} network becomes smaller, which helps to reduce V_{ss} noise. This V_{ss} noise suppression has been reported with simulation in [3]–[5] and measurement [5].

A triple-well structure is modeled as shown in Fig. 2. V_{dd} and V_{ss} are connected to the deep n-well and p-well respectively. There is also a resistance network of substrate under the deep n-well. In case of the triple-well structure, there are two types of well junction capacitance, which are capacitance between p-well and deep n-well (C_{pwj}), and
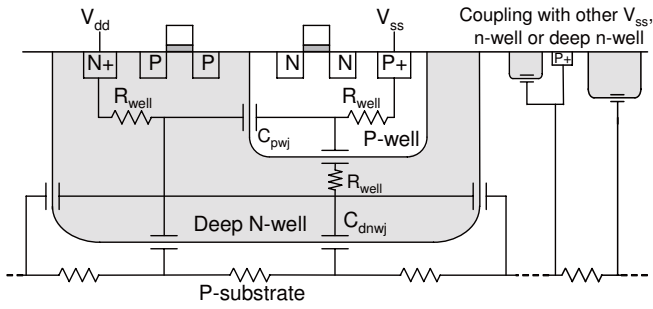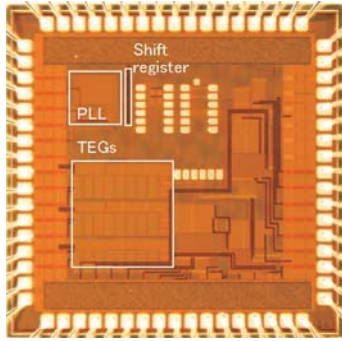
Fig. 2. Parasitic capacitance of deep n-well structure.

Fig. 3. Micrograph of the test chip. Chip size is $2.5 \times 2.5 \text{mm}^2$.

capacitance between deep n-well and p-substrate (C_{dnwj}). Both C_{pwj} and C_{dnwj} help to stabilize V_{dd}. In contrast, V_{ss} receives benefit only of C_{pwj}.

There are two aspects in terms of power supply and ground noises in the triple-well structure. The first aspect is that V_{ss} noise increases since the resistive network of substrate no longer helps to stabilize V_{ss}, which may deteriorate power supply noise significantly. On the other hand, as for V_{dd} network, PN junction capacitance associated with the triple-well structure increases to $C_{dnwj} + C_{pwj}$, whereas it is C_{nwj} only in the twin-well structure. Therefore, another aspect is that V_{dd} noise is alleviated by the increased junction capacitance. It is not clear which is dominant, decrease in V_{dd} noise or increase in V_{ss} noise, and whether the power supply noise increases, decreases or unchanged in total. To clarify this point is the objective of this work, and we will reveal it with measurement and simulation results in the following sections.

III. MEASUREMENT CIRCUIT STRUCTURE

A. Overview of test chip

A test chip for evaluating substrate and deep n-well effects on power supply noise was fabricated with a 90nm CMOS process. Figure 3 shows a micrograph of the test chip. The measurement circuit on the test chip consists of TEGs, shift registers, and PLL. Power supply noise is induced, and V_{dd} and V_{ss} waveforms are observed on TEGs. The PLL supplies a clock signal to TEGs. The shift registers store configurations of TEGs and PLL. The counter used in the waveform sampling macro is also included in the shift registers.
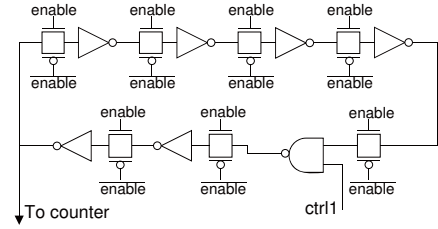
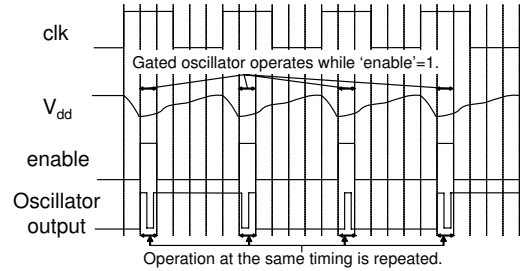

Fig. 4. Waveform sampling macro.
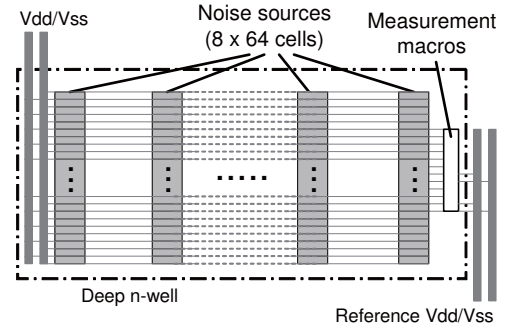

Fig. 5. Operation of waveform sampling macro.

Fig. 6. Layout of noise sources and measurement macros.

B. Circuit for waveform sampling

We adopt a ring oscillator-based macro previously proposed in [8] for capturing V_{dd} and V_{ss} waveforms. Figure 4 shows the structure of waveform sampling macro. This macro includes a ring oscillator consisting of inverters and transmission gates, and the transmission gates stop the operation of the ring oscillator. Figure 5 explains measurement operation of this macro. An ordinary ring oscillator without transmission gates operates continuously, and thus the supply voltage at a specific timing cannot be observed. This macro in Fig. 4 operates only while the timing range of interest, and the state of the macro is held during other timing ranges. This macro captures supply voltage of specific timing range. This macro senses and outputs variation of supply voltage as cycle count variation of the ring oscillator. The circuit repeatedly senses the supply voltage at the same timing, and the voltage is computed from the cycle count stored in the counter. This operation is repeated sweeping the sensing timing, and finally the waveform is obtained.

C. TEG structure

Each TEG consists of a DUT with noise sources and the measurement macros, and a control logic. Figure 6 shows the layout of the DUT and measurement macros. The noise
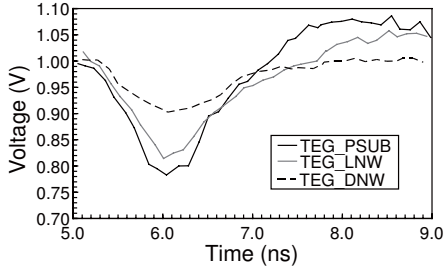
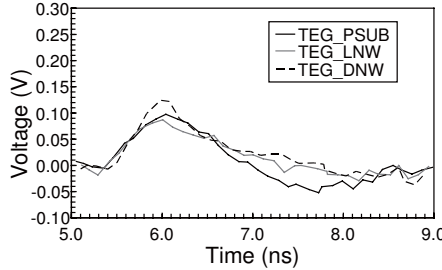Fig. 7. Measured V_{dd} waveforms. V_{dd} noise in TEG_DNW is smaller than that of TEG_PSUB.

Fig. 8. Measured V_{ss} waveforms. Increase of V_{dd} noise in TEG_DNW is relatively small in comparison with reduction of V_{dd} noise.
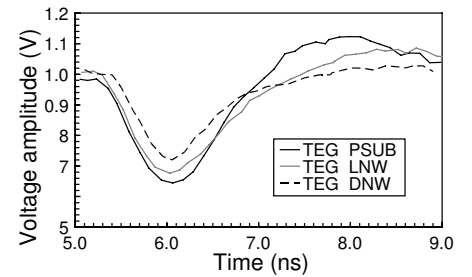

Fig. 9. Measured waveforms of voltage amplitude ($V_{dd} - V_{ss}$). Power supply noise is reduced in TEG_DNW

sources are 512 cells of 12-stage NAND gates. 64 noise sources are placed as a column with 76.72μm pitch in 620μm$\times 160\mu$m DUT area, and their density in DUT is 22%. To observe V_{dd} waveform, V_{ss} waveform, and waveform of V_{dd} and V_{ss} difference separately, three measurement macros are integrated. The first macro is connected to V_{dd} of the DUT and a dedicated stable reference V_{ss}, the second one to a dedicated stable reference V_{dd} and V_{ss} of the DUT, and the last one to V_{dd} and V_{ss} of the DUT.

We implemented three TEGs named TEG_PSUB, TEG_LNW, TEG_DNW. The DUT is isolated by the deep n-well as shown in Fig. 6 in TEG_DNW. In TEG_PSUB, TEG_LNW, the DUTs are implemented on p-substrate The n-well area in TEG_LNW is five times larger than that in TEG_PSUB. V_{dd} and V_{ss} of each TEG are directly connected to package pins, and are not shared with other TEGs.

IV. MEASUREMENT RESULTS

We measured V_{dd}, V_{ss}, and V_{dd}-V_{ss} waveforms of TEG_PSUB, TEG_LNW and TEG_DNW, when all noise sources operate with 100MHz clock signal. Figures 7, 8, and 9 show measured waveforms. The enable pulse of the sampling macros whose width is 200ps is swept by 100ps for capturing waveforms. The voltage resolution is 10mv in this configuration.

Voltage drop in TEG_LNW is smaller than that in TEG_PSUB as we expected because of increased well junction capacitance. This result indicates that well junction capacitance works as decoupling capacitance.

We next examine the substrate and deep n-well effect on V_{dd} and V_{ss} noises. V_{ss} noise of TEG_DNW is larger than that of TEG_PSUB in Fig. 8, as discussed in Sec. II. This result confirms that the resistive network of the p-substrate reduces V_{ss} noise, and this noise suppression effect weakens in the deep n-well structure. Figure 7 shows that V_{dd} noise of TEG_DNW is smaller than that of TEG_PSUB, and we observed that C_{dnwj} associated with the deep n-well notably reduces V_{dd} noise. V_{dd}-V_{ss} waveform in Fig. 9 demonstrates that the voltage drop given to the operating circuit is the smallest in TEG_DNW. This result means that the V_{dd} noise reduction thanks to C_{dnwj} overwhelms the increase in V_{ss} noise in the triple-well structure. Our measurement results clearly indicated that the deep n-well structure can alleviate power supply noise in comparison with ordinary p-substrate
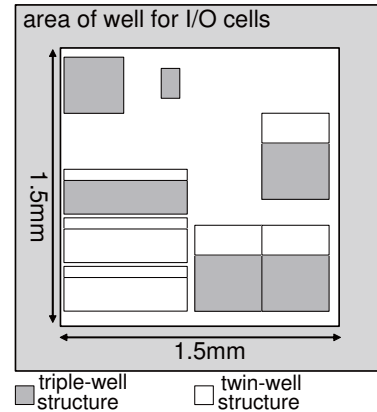

Fig. 10. Layout of n-well, deep n-well, and well of I/O cells on the test chip considered in simulation.
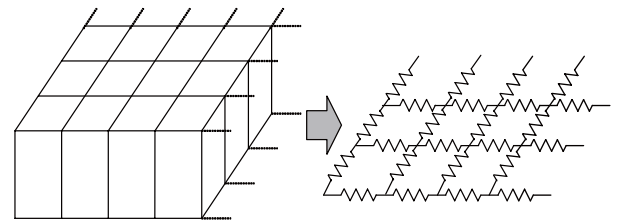

Fig. 11. 2D substrate mesh.

structure. The role of parasitic capacitance involved with the deep n-well is important for simulation, and neglecting this effect can cause overestimation of supply noise.

V. SIMULATION CONSIDERING SUBSTRATE AND WELL

This section shows simulation results considering substrate and well structures, and verifies the noise suppression effects. We adopt a simple simulation modeling to validate the measured supply noise variation.

A. Simulation setup

We simulate power supply and ground noises with a circuit simulator [10]. The simulated circuit includes full-chip power and ground distribution network, noise sources, package and bonding wires, full-chip substrate, and all wells on the chip. The layout outline of these components on the test chip is depicted in Fig. 10. The substrate of 1.5×1.5mm^2 chip area, which is used for implementation of core circuit, is modeled as a 100μm-pitch 2D resistive mesh shown in Fig. 11.
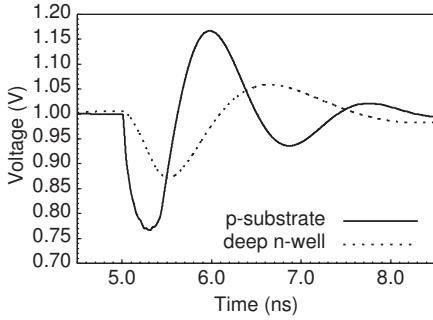
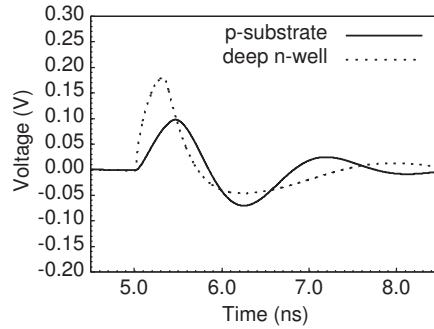Fig. 12. V_{dd} waveforms in simulation. Reduction of peak V_{dd} noise due to substrate is simulated.

Fig. 13. V_{ss} waveforms in simulation. V_{ss} noise increases in triple-well structure.
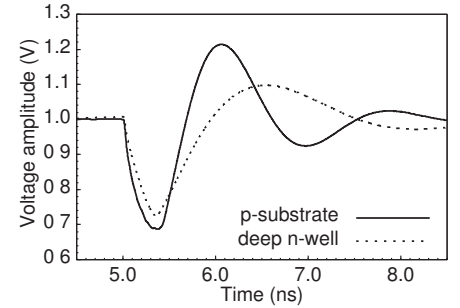
Fig. 14. V_{dd}-V_{ss} waveforms in simulation. Reduction of power supply noise is simulated similarly to the measurement result.

Power supply network is modeled with package inductance and on-chip resistance. The noise source circuit in a TEG of interest is modeled with variable switch model proposed in [9] to make simulation time practical.

PN junction capacitances of n-well and deep n-well in the core area is connected to V_{dd}/V_{ss} supply network and substrate network considering their layout positions. The well junction capacitance of I/O cells are connected to the edges of the substrate mesh. We here omitted R_{well} for simplicity because RC time constant of PN junction capacitance is estimated to be sufficiently small.

Resistance and capacitance values are calculated from the process datasheet of the fabricated chip. Sidewall and bottom junction capacitances of the deep n-well are estimated to be three times large and the same as that of the n-well. Resistivity and depth of p-substrate are not given from a foundry, and are assumed to be 100mΩ/m and 100μm [11].

B. Simulation results and discussion

We simulated power supply and ground waveforms in the twin-well and triple-well structures. The given operating condition of noise source is the same as the measurement in Sec. IV. Simulated V_{dd}, V_{ss}, and V_{dd}-V_{ss} waveforms are shown in Figs 12, 13 and 14.

Peak V_{dd} drop is reduced by the deep n-well (Fig. 12), and V_{ss} drop is alleviated by the p-substrate (Fig. 13). Total V_{dd}-V_{ss} amplitude slightly decreases in the deep n-well structure (Fig. 14). The noise variation due to the p-substrate and deep n-well is well reproduced and correlated with the measurement results, though the circuit modeling is relatively simple.

These simulation results validate the measurement result of noise suppression effect by the p-substrate and deep n-well on the test chip. In addition, we demonstrated that the impact of p-substrate and deep n-well on V_{dd} and V_{ss} noises can be reasonably simulated by attaching a resistive substrate mesh and distributed well capacitances to the power distribution network.

VI. CONCLUSION

This paper observed remarkable effects of substrate and deep n-well on power supply on the 90nm test chip, and demonstrated that their effects can be explained by simulations with a relatively simple modeling of substrate and well capacitances. V_{ss} noise was mitigated by resistive p-substrate network. PN junction capacitance involved with triple-well structure also alleviated power supply noise. The triple-well structure slightly increases V_{ss} noise yet reduces V_{dd} noise more, and can improve power integrity in total.

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