Correlation Verification between Transistor Variability Model with Body Biasing and Ring Oscillation Frequency in 90nm Subthreshold Circuits

Hiroshi Fuketa[†*], Masanori Hashimoto[†*], Yukio Mitsuyama[†*], and Takao Onoye[†*]
[†]Dept. Information Systems Engineering, Osaka University, JAPAN [*]JST, CREST
{fuketa.hiroshi, hasimoto, mituyama, onoye}@ist.osaka-u.ac.jp

ABSTRACT

This paper presents modeling of manufacturing variability and body bias effect for subthreshold circuits based on measurement of a device array circuit in a 90nm technology. The device array consists of P/NMOS transistors and ring oscillators. This work verifies the correlation between the variation model extracted from I-V measurement results and oscillation frequencies, which means the transistor-level variation model is examined and confirmed in terms of circuit performance. We demonstrate that delay variations of subthreshold circuits are well characterized with two parameters - threshold voltage and subthreshold swing parameter. We reveal that body bias effect is a less statistical phenomenon and threshold voltage shift by body biasing can be modeled deterministically.

Categories and Subject Descriptors

B.7.0 [**Integrated Circuits**]: General

General Terms

Design, Measurement, Verification

Keywords

subthreshold circuit, manufacturing variability, body biasing

1. INTRODUCTION

For ultra-low power applications, various subthreshold circuits have been proposed [1, 2]. Subthreshold circuits operate at lower supply voltage than threshold voltage (V_{th}) of MOSFETs. In this region, drain current has exponential dependence on V_{th}, which means the circuit delay is significantly sensitive to manufacturing variability. However, characterization of manufacturing variability focusing on subthreshold circuits has not been reported, whereas the subthreshold leakage current has been measured for estimating static power variation [3].

Circuits for measuring transistor variations have been proposed [3–6]. [3] and [4] proposed device array circuits and measured the variation of V_{th}. [5] described V_{th} isolation from measured data using the equation of MOSFET I-V characteristics. In [6], the variations of the channel length and thickness of gate oxide are extracted from leakage currents of transistors and RO frequencies. In these papers, however, the impact of these variations on subthreshold circuits is not clearly discussed. The correlation between subthreshold current modeling and performance of subthreshold circuits has not been verified, as far as the authors know.

Subthreshold circuits are sensitive to manufacturing variability, as mentioned above. Therefore, post-silicon compensation techniques are indispensable for subthreshold circuits to meet the required performance of speed and power dissipation. As one of the possible techniques, body biasing has been proposed [7, 8]. The variation of V_{th} with body bias has been studied [9–11]. These papers show that forward body bias (FBB) improves the standard deviation of V_{th} and reverse body bias (RBB) deteriorates that of V_{th} in comparison to zero body bias (ZBB). However, the circuit delay with body bias for subthreshold circuits has not been discussed.

This work is the first work that explicitly verifies the correlation between device variability modeling and performance variation of subthreshold circuit considering body biasing. We reveal that distributions of V_{th} and subthreshold swing parameter extracted from measurement results well reproduce the distribution of measured RO frequencies. The measurement results show that the V_{th} shift by body biasing depends on V_{th}, but it can be deterministically modeled. For evaluating this correlation, we designed and fabricated a device array circuit with variable body voltage which alternately placed MOSFETs for measuring their I-V characteristics and ring oscillators (ROs) in a 90nm technology.

The reminder of this paper is organized as follows. Section 2 describes the device array circuit. Section 3 demonstrates measurement results of the device array circuit and variability characterization. In section 4, we discuss the variation with body bias. Finally, section 5 concludes the paper.

2. DEVICE ARRAY CIRCUIT

2.1 Circuit Structure Overview

Figure 1 shows the device array circuit designed to measure variations of MOSFET I-V characteristics and RO frequencies in subthreshold region. The device array consists of 100×16 blocks. Each block contains two NMOSs and two PMOSs for measuring their I-V characteristics and an 11-stage RO. It is possible to evaluate a correlation between MOSFET I-V characteristics and RO frequencies by placing MOSFETs and ROs in the same area. The body voltage of MOSFETs and ROs can be changed. In addition, 23-stage and 47-stage ROs are integrated to reveal a relation between a logic depth and variation of RO frequencies.

A test chip in Fig. 2 was fabricated in a 90nm CMOS process with six metal layers and triple-well structure, and the device array circuit with the control logic and the micro pads occupies 2.25mm $\times$ 0.68mm area. Table 1 lists the device count in the device array circuit.

ISLPED'08, August 11–13, 2008, Bangalore, India..

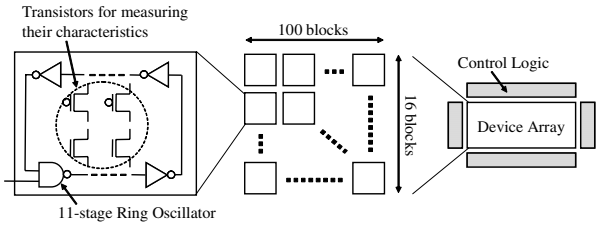


Figure 1: Device array structure.

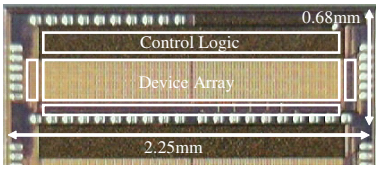


Figure 2: Micrograph of the test chip.

2.2 Measurement Circuit for MOSFET characteristics

Figure 3 shows the measurement circuit for MOSFET I-V characteristics. For measuring small subthreshold currents accurately, we designed the circuit based on the transistor array circuit proposed in [3]. We improved [3] such that both PMOS and NMOS characteristics can be measured. In addition, the body bias of MOSFETs is changeable in the designed array. In Fig. 3, VPW is the body voltage of NMOS and VNW is that of PMOS.

The transistor for measuring its I-V characteristics is selected by a column selection signal and a row selection signal. Force and sense pins of drain, gate, and source can be used for Kelvin connection in order to eliminate influence of the parasitic wire resistances. Drains and gates of the transistors in the selected column are connected to the drain and gate force pins to which drain voltage and gate voltage are applied. Drains and gates of the transistors in the unselected columns are connected to the clamp pins. Sources of the transistors in the selected row are connected to the force pin to which source voltage is applied. Sources of the transistors in the unselected rows are connected to the sink pin. The voltages of the drain clamp and sink pins are set to 0V. The voltage of the gate clamp pin is adjusted to minimize the leakage currents of unselected transistors. I-V characteristics of the selected transistor can be measured by observing the current in the source force pin.

2.3 Measurement Circuit for Ring Oscillator Frequencies

Figure 4 shows the measurement circuit for RO frequencies. VDD and GND of ROs in the unselected columns are connected to the clamp pin whose voltage is set to 0V. The selector consists of tri-state buffers with the hierarchical structure to ensure the operation in subthreshold region [2]. The circuit is designed such that body bias of ROs can be changed. The output of RO is divided by 1,024.

3. MEASUREMENT RESULTS AND CHARACTERIZING VARIATIONS

3.1 Variation of RO Frequencies

Table 2 lists standard deviation / mean (σ/μ) of measured 11-stage, 23-stage and 47-stage RO frequencies at V_{DD}=0.3V. σ/μ is nearly proportional to $1/\sqrt{N}$ where N is the number of RO stages (Fig. 5). If the delay variation of the inverters in RO is completely

Table 1: Device count in the device array circuit.

NMOS	3,200
PMOS	3,200
11-stage RO	1,600
23-stage RO	800
47-stage RO	400

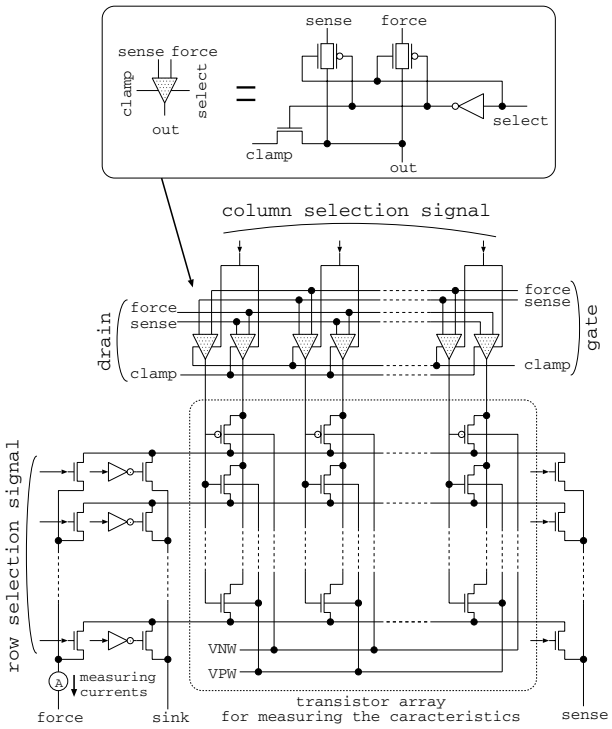


Figure 3: Measurement circuit for MOSFET I-V characteristics.

random and independent, σ/μ is proportional to $1/\sqrt{N}$. This relation indicates that a random variation is dominant in the delay variation of subthreshold circuits. For designing subthreshold circuits, random variation of devices should be considered as a primary concern.

3.2 Characterizing Variations

We here discuss how to model MOSFET variations from measured I-V characteristics. The drain current I_{ds} in subthreshold region is expressed as follows in BSIM4 model [12].

$$I_{ds} = I_0 \mathrm{e}^{\frac{V_{ds}-V_{th}-V_{off}}{nV_t}} \left(1 - \mathrm{e}^{-\frac{V_{ds}}{V_t}}\right), \quad (1)$$

where

$$I_0 = \mu \frac{W}{L} \sqrt{\frac{q\varepsilon_{\mathrm{si}}\mathrm{NDEP}}{2\Phi_s}} V_t^2. \quad (2)$$

n is the subthreshold swing parameter, V_{off} is the offset voltage, V_t is the thermal voltage, $\varepsilon_{\mathrm{si}}$ is the dielectric constant of Si, NDEP is the doping concentration, and Φ_s is the surface potential. In (1), $\mathrm{e}^{\frac{V_{ds}-V_{th}-V_{off}}{nV_t}}$ term is dominant. [3] reports that n as well as V_{th} are varied. We thus consider manufacturing variability of both V_{th} and n in this work in order to characterize variations accurately.

We derive V_{th} and n from the measured I-V characteristics such

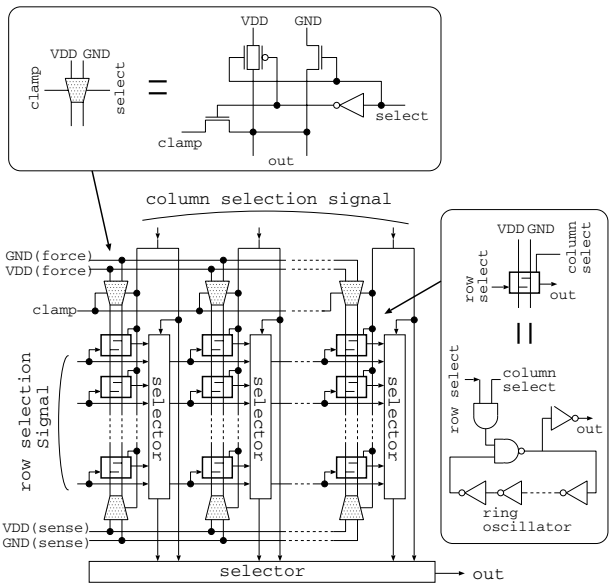


Figure 4: Measurement circuit for RO frequencies.

Table 2: Relation between number of stages and frequencies of ROs (V_{DD} = 0.3V).

number of stages	Frequencies (divided by 1,024)		
	μ [KHz]	σ [KHz]	σ/μ [%]
11	24.7	1.9	7.6
23	11.7	0.63	5.3
47	5.89	0.22	3.8

that the sum of relative errors at 7 measurement points between the measured and simulated currents is minimized by numerical fitting.

A parameter of DELVTO is used to change V_{th}. On the other hand, it is impossible to change n directly. We, in this work, use a parameter of NFACTOR to represent n variation. Subthreshold swing parameter n is expressed in BSIM4 as follows.

$$n = 1 + \text{NFACTOR} \cdot \frac{C_{\text{dep}}}{C_{\text{oxe}}} + \frac{\text{Cdsc\_Term} + \text{CIT}}{C_{\text{oxe}}}. \qquad (3)$$

C_{oxe} is the gate oxide capacitance, C_{dep} is the depletion-layer capacitance, Cdsc_Term is the coupling capacitance, and CIT is the interface trap capacitance. NFACTOR is originally introduced as an empirical parameter to compensate for errors in calculating depletion width capacitance [12].

Figure 6 shows an example of measured and simulated I_{ds}-V_{gs} characteristics at V_{ds}=0.3V with the extracted DELVTO and NFACTOR parameters. For a comparison, we extracted DELVTO parameter solely assuming NFACTOR parameter is constant. The simulation result corresponding to this single parameter modeling with DELVTO is also shown in Fig. 6. In terms of ON current (V_{ds}=V_{gs}=0.3V), the error between the measurement result and the simulation result of DELVTO modeling is 24%, whereas it improves to 9% in the simulation with DELVTO and NFACTOR modeling.

Performing the extraction for all transistors, we can obtain the distributions of DELVTO and NFACTOR variations that express V_{th} and n variations. Figure 7 shows the distribution of DELVTO parameter corresponding to V_{th} variation when V_{ds}=0.3V. Figure 8 shows the distribution of NFACTOR parameter corresponding to n variation when V_{ds}=0.3V. Both NMOS V_{th} and PMOS V_{th} are normally distributed. σ of NMOS V_{th} is bigger than σ of PMOS

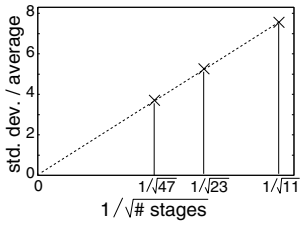


Figure 5: Number of stages versus σ/μ of RO frequencies.

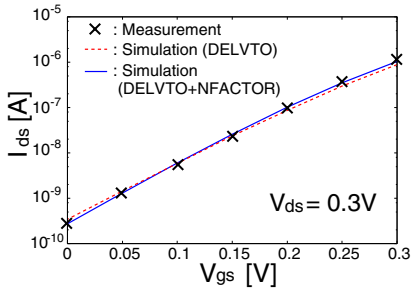


Figure 6: An example of measured and simulated I-V characteristics.

V_{th} because the channel width of NMOS is smaller than that of PMOS by 35%.

In handling measurement data, exclusion of outliers is critically important to make a reasonable statistical model, since some outliers lead the average and standard deviation to totally inappropriate values. In this paper, we excluded these values using subthreshold swing parameter n. n can be calculated from the measured data according to equation (1). We define n as a slope between V_{gs}=0.05V and 0.15V at V_{ds}=0.3V for NMOS, and V_{gs}=$-$0.15V and $-$0.05V at V_{ds}=$-$0.3V for PMOS. Figure 9 shows the distribution of n calculated from the measured data. In 96% of PMOSs, n is no more than 1.6 and the rest widely spreads. For example, Fig. 10-a shows the measured and simulated results with DELVTO and NFACTOR modeling for a PMOS with n=1.55. The normalized NFACTOR is 1.14, and the average error between them is 7.4%. Figure 10-b shows the measured and simulated results for a PMOS with n=1.7, where the lower bound of the normalized NFACTOR is set to 1.1 in the parameter fitting according to Fig. 8. In this case, the average error is 18%, and the current is not modeled well. Without the lower bound of the normalized NFACTOR, the average error could be improved, but the normalized NFACTOR jumps to 0.94, which is much distant from the distribution in Fig. 8. This means it is difficult to reproduce I-V characteristics of large n transistors by BSIM4 model with DELVTO and NFACTOR parameters. Thus, we exclude the transistors of $n > 1.6$ in this paper. One NMOS (0.03%) and 125 PMOSs (4%) in the device array are excluded.

Finally, we discuss the correlation coefficients between the two parameters. The correlation coefficient between DELVTO and NFACTOR of NMOS is 0.042 and that of PMOS is 0.069. The correlation coefficient between NMOS and PMOS of DELVTO is 0.016 and that of NFACTOR is 0.0025. All the correlation coefficients are below 0.1, therefore we consider the distributions have almost no correlation. The following assumes DELVTO and NFACTOR are normally distributed with no correlation.

3.3 Evaluation of Variation Model

To validate the variation model constructed in section 3.2, we perform circuit simulations and obtain RO frequencies with the

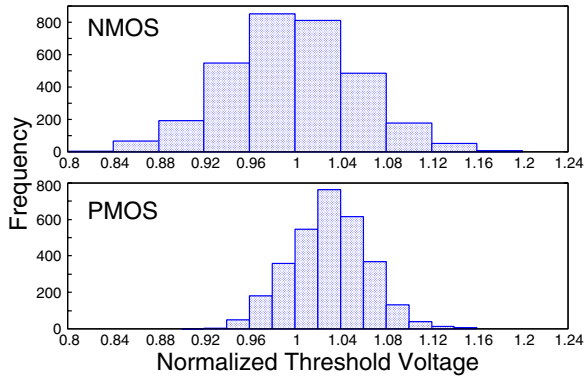


Figure 7: Distribution of DELVTO parameter corresponding to V_{th} variation.

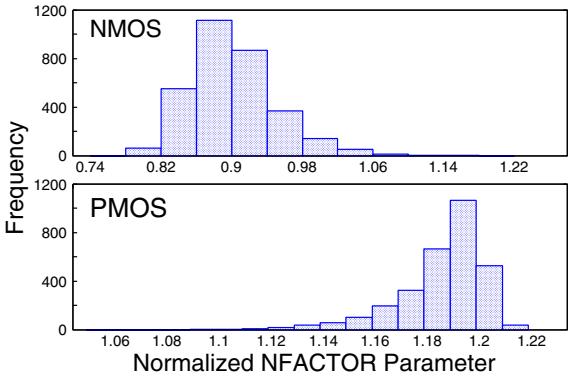


Figure 8: Distribution of NFACTOR parameter corresponding to n variation.

variation model, and then compare the simulation results to the measurement results.

Figure 11 shows the distributions of 11-stage RO frequencies (Fig.11-a) and 47-stage RO frequencies (Fig.11-b) which are obtained by Monte Carlo simulations (1,000 runs) with DELVTO and NFACTOR modeling, and with DELVTO modeling. The parasitic capacitances and resistances are extracted by Star-RCXT. Table 3 shows the average (μ) and standard deviation (σ) of RO frequencies. In both 11-stage and 47-stage ROs, the distribution simulated with DELVTO and NFACTOR modeling is much closer to the measurement. The average frequency is underestimated by 16% when modeling variation with DELVTO only, whereas it is well estimated within 6% error when both variations of DELVTO and NFACTOR are modeled. This means that accurate variational analysis of subthreshold circuits can be performed with variation models of V_{th} and subthreshold swing parameter n.

4. EVALUATION OF BODY BIAS EFFECT

This section discusses body biasing based on the measurement results of I-V characteristics and RO frequencies. We explain the modeling of body bias effect in subthreshold circuits, and evaluate the model.

4.1 Measurement Results

We measured I_{ds}-V_{gs} characteristics at V_{ds}=0.3V with 0.3V FBB (Forward Body Bias). From the measurement results, DELVTO and NFACTOR are extracted similarly to section 3. Table 4 shows the average (μ) and the standard deviation (σ) of V_{th} at ZBB (Zero

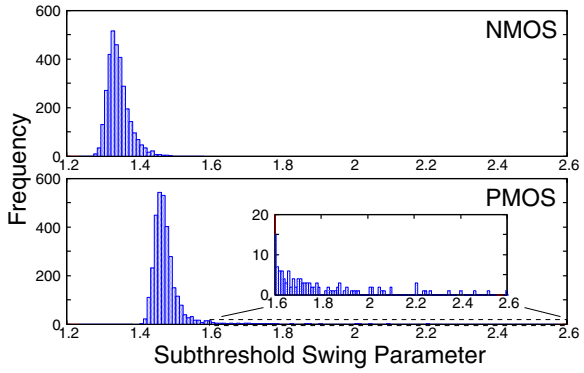
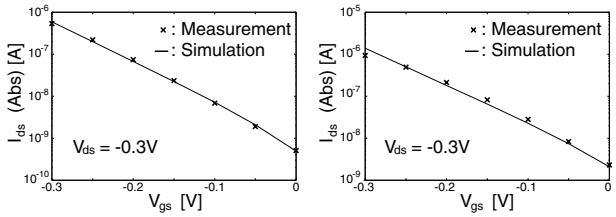


Figure 9: Subthreshold swing parameter calculated n from measured data.



(a) n=1.55 (b) n=1.7

Figure 10: Measured and simulated I-V characteristics for PMOS.

Body Bias) and FBB. With 0.3V FBB, μ and σ of NMOS V_{th} decrease by 15% and 20% respectively. μ and σ of PMOS V_{th} decrease by 19% and 17% at 0.3V FBB. These results are consistent with the analysis for super-threshold circuits in previous work [9, 10].

We also measured RO frequencies at V_{DD}=0.3V with 0.3V FBB and 0.3V RBB. Table 5 and Fig. 12 show μ and σ of 23-stage and 47-stage RO frequencies with ZBB, 0.3V FBB, and 0.3V RBB. μ of both 23-stage and 47-stage RO frequencies at 0.3V FBB is 3.6× faster than that at ZBB, and σ/μ improves by around 1%. On the other hand, μ of both 23-stage and 47-stage RO frequencies at 0.3V RBB is smaller than that at ZBB by 70%, and σ/μ deteriorates by 1%. FBB improves not only circuits delay but also their variation, whereas RBB deteriorates circuit delay and its variation.

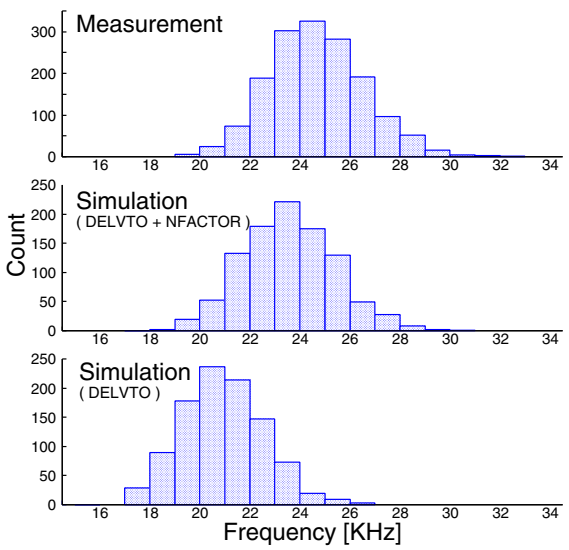
4.2 Modeling of Body Bias Effect

We here examine whether body bias effect has variation, i.e. V_{th} shift with body biasing should be modeled statistically or deterministically.

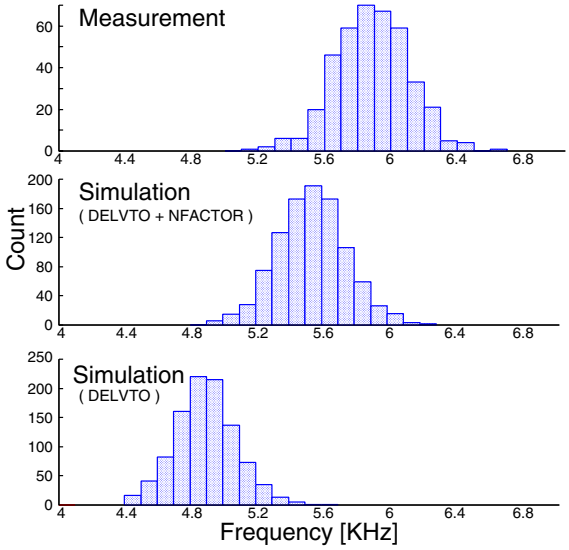
Figure 13 shows the body bias effect and each dot corresponds to each transistor in the device array, where the horizontal axis is V_{th}(@ ZBB) and the vertical axis is V_{th}(@ FBB) divided by V_{th}(@ ZBB). The ratio of V_{th}(@ FBB) to V_{th} (@ ZBB) is almost constant regardless of V_{th}(@ ZBB). We here suppose that V_{th}(@ FBB) can be expressed as

$$V_{th}(\text{@ FBB}) \quad = \quad \alpha \cdot V_{th}(\text{@ ZBB}). \qquad (4)$$

From the measurement results in Fig. 13, α can be regarded as a constant. α of NMOS is 0.85 and α of PMOS is 0.81. This means that both μ and σ of V_{th} variation at FBB are α times as small as those at ZBB. Thus, σ/μ is constant, which is consistent with the measurement results in Table 4. Rigidly speaking, α fluctuates little, and the standard deviations of α of NMOS and PMOS are



(a) 11-stage RO



(a) 47-stage RO

Figure 11: Measurement and simulation of RO frequencies (V_{DD}=0.3V).

Table 3: Average and standard deviation of RO frequencies (V_{DD}=0.3V).

		Frequencies (divided by 1,024)		
		μ [KHz]	σ [KHz]	σ/μ [%]
11-stage RO	Measurement	24.7	1.9	7.6
	Simulation (DELVTO+NFACTOR)	23.6	1.8	7.7
	Simulation (DELVTO)	20.9	1.6	7.9
47-stage RO	Measured	5.89	0.22	3.8
	Simulation (DELVTO+NFACTOR)	5.54	0.21	3.8
	Simulation (DELVTO)	4.89	0.18	3.8

Table 4: Average and standard deviation of V_{th} with body bias.

		$\mu(V_{th})$	$\sigma(V_{th})$	σ/μ
NMOS	ZBB	1	1	1
	FBB (0.3V)	0.85	0.80	0.94
PMOS	ZBB	1	1	1
	FBB (0.3V)	0.81	0.83	1.02

0.01 and 0.01. We think this fluctuation mainly comes from measurement and fitting errors, and V_{th} variation due to this is small enough to be ignored compared to manufacturing variability.

To verify the body bias model discussed above, we compare RO frequencies simulated with the model and the measurement results. In the simulation, DELVTO at FBB is computed with (4), and given to the simulator. For instance, a NMOS with DELVTO=10mV at ZBB is modified to NMOS with DELVTO=8.5mV at FBB. As for NFACTOR, the offset caused by body biasing, which is the average difference between NFACTORs at ZBB and FBB, is added to NFACTOR at ZBB. Rigidly speaking, the offset has a distribution, however, NFACTOR is the secondary effect and then NFACTOR is shifted uniformly for simplicity.

Table 6 shows a comparison between the measured and simulated RO frequencies at V_{DD}=0.3V with 0.3V FBB. The number of runs in Monte Carlo simulation is 1,000. The average frequency (μ) is estimated with 11% error, and the variation (σ/μ) is almost

Table 5: Average and standard deviation of RO frequencies with body bias (V_{DD}=0.3V).

		Frequencies (divided by 1,024)		
		μ [KHz]	σ [KHz]	σ/μ [%]
23-stage RO	FBB (0.3V)	41.8	1.6	3.8
	ZBB	11.7	0.63	5.3
	RBB (0.3V)	3.49	0.23	6.6
47-stage RO	FBB (0.3V)	21.0	0.55	2.7
	ZBB	5.89	0.22	3.8
	RBB (0.3V)	1.76	0.23	4.9

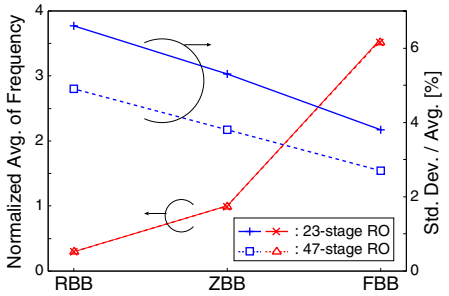


Figure 12: μ and σ/μ of RO frequencies with body bias.

the same. We think that the average difference is caused by the dependency of the depletion capacitance on the body voltage, because FBB is not supported in the original model card given from the foundry.

Figure 14 shows measured and simulated RO frequencies. The horizontal axis is the measured/simulated RO frequency at ZBB. The vertical axis is the speed-up due to FBB which is defined as the measured/simulated RO frequency at FBB divided by the measured/simulated RO frequency at ZBB. The measurement result shows that RO frequency at FBB is 3.6 times higher than that at ZBB when V_{DD}=0.3V. In the simulation results, FBB multiplies RO frequencies by 4.1. The speed-up thanks to FBB is well estimated in Fig. 14, though there is an offset. We think this is because the increase in depletion capacitance to body is not considered in

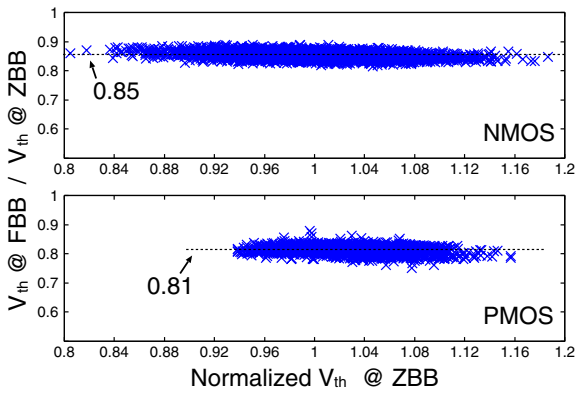


Figure 13: Relation between V_{th} at ZBB and V_{th} at FBB / V_{th} at ZBB.

Table 6: Measured and simulated 23-stage RO frequencies with 0.3V FBB (V_{DD}=0.3V).

	Frequencies (divided by 1,024)		
	μ [KHz]	σ [KHz]	σ/μ [%]
Measurement	41.8	1.6	3.8
Simulation	46.4	1.8	3.9

the simulation, and then the speed-up is overestimated in the simulation, which is similar to Table 6.

We in this section conclude that deterministic modeling of V_{th} shift due to body biasing provides accurate estimation of RO frequency variation.

5. CONCLUSION

This work discusses correlation between variation model in transistor model card and ring oscillation frequency as a primary metric of circuit performance. To characterize variations of subthreshold circuits, we designed the device array circuit, and measured the variation of MOSFET I-V characteristics and RO frequencies. We demonstrated that modeling variations of I-V characteristics with V_{th} and subthreshold swing parameter n accurately estimates delay variations of subthreshold circuits.

We also examined V_{th} shift due to body biasing. The measurement results showed that FBB improves not only circuits delay but also their variation, whereas RBB worsens both. We revealed that V_{th} shift due to body bias can be modeled deterministically, and demonstrated that the delay variations of subthreshold circuits with FBB can be estimated with the deterministic body bias model and distributions of V_{th} and subthreshold swing parameter n.

6. ACKNOWLEDGMENTS

The VLSI chip in this study has been fabricated through the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo, with the collaboration by STARC, Fujitsu Limited, Matsushita Electric Industrial Company Limited., NEC Electronics Corporation, Renesas Technology Corporation, and Toshiba Corporation. This study was partly supported from NEDO of Japan.

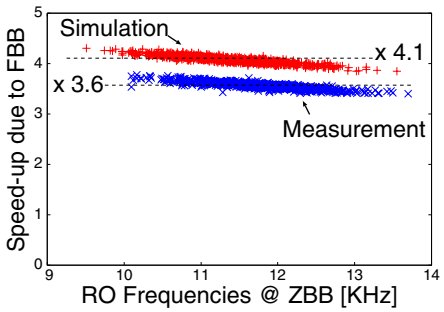


Figure 14: Relation between 23-stage RO frequencies at ZBB and speed-up. Speed-up is defined as RO frequencies at FBB / those at ZBB.

7. REFERENCES

[1] A.W. Wang, B.H. Calhoun, and A.P. Chandrakasan, "Sub-threshold Design For Ultra Low-Power Systems," Springer, NEY YORK, 2006.

[2] A.W. Wang and A.P. Chandrakasan, "A 180-mV Subthreshold FFT Processor Using a Minimum Energy Design Methodology," *IEEE J. Solid-State Circuits*, vol.40, pp.310–319, Jan. 2005.

[3] K. Agarwal, et al., "A Test Structure for Characterizing Local Device Mismatches," in *Int. Symp. on VLSI Circuits Dig. Tech. Papers*, pp.67–68, Jun. 2006.

[4] S. Ohkawa, et al., "Analysis and Characterization of Device Variations in an LSI Chip Using an Integrated Device Matrix Array," *IEEE Trans. Semiconductor Manufacturing*, vol.17, pp.155–165, May. 2004.

[5] N. Drego, A. Chandrakasan, and D. Boning, "A Test-Structure to Efficiently Study Threshold-Voltage Variation in Large MOSFET Arrays," in *Proc. Int. Symp. Quality Electronic Design*, pp.281–286, Mar. 2007.

[6] L.T. Pang and B. Nikolic, "Impact of Layout on 90nm CMOS Process Parameter Fluctuations," in *Int. Symp. on VLSI Circuits Dig. Tech. Papers*, pp.69–70, Jun. 2006.

[7] J.W. Tschanz, et al., "Adaptive Body Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations on Microprocessor Frequency and Leakage," *IEEE J. Solid-State Circuits*, vol.37, pp.1396–1402, Nov. 2002.

[8] S. Hanson, et al., "Performance and Variability Optimization Strategies in a Sub-200mV, 3.5pJ/inst, 11nW Subthreshold Processor," in *Int. Symp. on VLSI Circuits Dig. Tech. Papers*, pp.152–153, Jun. 2007.

[9] D. Levacq, et al., "Spatial Frequency Analysis of Intra-Die Variations with 4-mm 4000 x 1 Transistor Arrays in 90nm CMOS," in *Proc. Custom Integrated Circuits Conference*, pp.257–260, Sep. 2007.

[10] Y. Komatsu et al., "Substrate-noise and random-fluctuations reduction with self-adjusted forward body bias," in *Proc. Custom Integrated Circuits Conference*, pp.35–38, Sep. 2005.

[11] A. Keshavarzi et al., "Measurements and modeling of intrinsic fluctuations in MOSFET threshold voltage," in *Proc. Int. Symp. on Low Power Electronics and Design*, pp.26–29, Aug. 2005.

[12] BSIM4 (Berkeley Short-channel IGFET Model 4), "http://www-device.eecs.berkeley.edu/bsim3/bsim4.html"