Clock Skew Evaluation Considering Manufacturing Variability in Mesh-Style Clock Distribution

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Abstract

Influence of manufacturing variability on circuit performance has been increasing because of finer manufacturing process and lowered supply voltage. In this paper, we focus on mesh-style clock distribution which is believed to be effective for reducing clock skew, and we evaluate clock skew considering manufacturing and design variabilities. Considering MOS transistor variation - random and spatially-correlated variation - and non-uniform flip-flop (FF) placement, we demonstrate that spatially-correlated variation and severe non-uniform FF distribution can be major sources of clock skew. We also examine the dependency of clock skew on design parameters, and reveal that finer clock mesh does not necessarily reduce clock skew.

1. Introduction

High performance microprocessor design enforces us to intensively minimize clock skew. Smaller clock skew is desirable not only for shortening clock cycle but also for reducing delay elements inserted to satisfy hold time constraints. The constraint of clock skew is often given as 5-10% of the clock cycle [1]. The obstacles to satisfy the skew constraints are: (1) manufacturing variability and environmental fluctuation such as power supply noise and variation in temperature, (2) design imperfectness such as difference of wire length between clock source and FF and non-uniform FF placement. These obstacles cannot be completely eliminated, and thus we have to develop a design scheme for robust clock distribution.

Mesh-style clock distribution has been recognized as a robust structure, and is used for several high performance microprocessor designs [2, 3]. In SoC design, a property of small skew in mesh structure is exploited for power reduction by using smaller clock drivers [4]. Conventionally, the robustness of mesh structure against non-uniform FF placement has been focused and utilized. As for CAD area, efficient analysis methods are studied [5], because driver outputs are shunted with the mesh and conventional gate-level timing analyzers cannot be used for clock skew analysis.

Among manufacturing variabilities, the variability of transistor is reported to be more significant than that of wire [6]. Transistor variability is often decomposed into chip-to-chip, layout-dependent, random and spatially-correlated components [7]. The chip-to-chip variability component affects chip performance directly, however from a viewpoint of clock skew, its impact is a secondary effect. The layout-dependent component can be modeled in LPE (layout parameter extraction) and cell library design, though its modeling might be expensive. The random component follows a normal distribution, and affects clock skew. The spatially-correlated component is sometimes modeled such that the correlation coefficient of two devices is expressed as a function of the distance between them [8].

In this paper, we focus on a hybrid structure that consists of a tree for global distribution and a mesh for final clock distribution, and quantitatively reveal dominant variabilities that fluctuate clock skew. This work evaluates clock skew considering "static" variability that includes manufacturing variability and design imperfectness. The random and spatially-correlated components of transistors and non-uniform FF placement are considered in our analysis. We also evaluate clock skew changing two important design parameters of clock mesh, mesh pitch and driver strength, and examine the dependency on these design parameters.

This paper is organized as follows. Section 2 describes the feature of mesh-style clock distribution. Section 3 evaluates clock skew considering manufacturing variability. We show dominant variability sources, demonstrate an example that finer mesh does not necessarily minimize clock skew, and point out a possibility of low power clock distribution. We finally conclude the discussion in Section 4.

2. Mesh-style clock distribution

A hybrid clock distribution structure with a tree and a mesh as shown in Figure 1 is often used in high-performance microprocessor design [2, 3]. The mesh is a grid structure, and a shunt wire connects adjacent nodes. The shunt wire reduces the clock skew which would intrinsically yield when no shunt wires were inserted, because early and late clock arrivals are equalized [9]. The mesh-style clock distribution thus has a property of clock skew reduction. However, generally speaking, it requires and in-
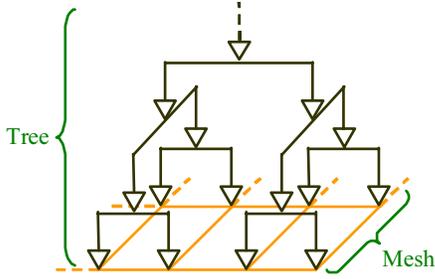
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Figure 1. Mesh-style clock distribution.
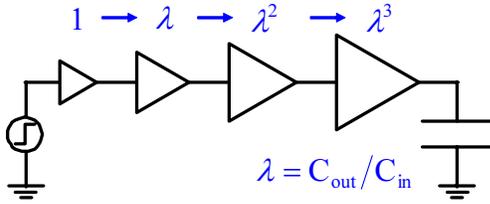

$$\lambda = C_{out}/C_{in}$$

Figure 2. Cascade driver.

volves much wire resource, wire capacitance, layout area, and power consumption. In addition, since nodes are connected to each other, conventional timing analysis cannot be applied, and the design verification including clock skew analysis needs long circuit simulation.

The clock distribution network usually has a large amount of load capacitance associated with large wire resistance, and then a number of buffers are inserted to avoid waveform distortion and reduce the latency from the source to the FFs. A cascade driver (Figure 2) is often used to drive a large load capacitance. The ratio λ of output capacitance C_{out} to input capacitance C_{in} is assigned to four to six [1].

3. Clock skew evaluation considering manufacturing variability

This section first explains the evaluation setup of clock distribution network and variability modeling. We then demonstrate experimental results.

3.1. Design of clock distribution network and its modeling for circuit simulation

The clock distribution structure used for the experiment is the hybrid structure with a H-tree and a mesh shown in Figure 1. We here assume a clock distribution within a 1mm square clock domain in an industrial 90nm technology. The mesh pitch is 100μm and the mesh is constructed with intermediate wires. The wiring material is copper, and we calculate the wire capacitance and resistance by given process information from the foundry. The wires are modeled

by π ladder circuit as shown in Figure 3 for circuit simulation. For a convenience, the mesh wire is segmented for every 1μm, and each segment is represented as a π ladder circuit. The wires in the tree and the wires from the mesh to FFs are modeled by 3π ladder circuits. The width of the mesh and tree wire is 0.64μm, and that of the mesh to FFs wire is 0.14μm.

H-tree structure, which is symmetrically branched, is used for the tree that drives the mesh. Each mesh node is driven by a final-stage driver, and the H-tree delivers clock signal to the final-stage drivers. In this experiment, clock drivers are inserted in every two branches of H-tree. We adopted the driver sizes of $\lambda = C_{out}/C_{in} = 5$ assuming FF placement is uniform, which means that the drivers at the same stage have the same size.

3.2. Experimental condition

We used a transistor model developed so that the current characteristics are compatible with the prediction in ITRS 2005 roadmap [10]. Clock skew for the fall clock edge is evaluated in Monte Carlo manner. We prepared 300 sets of manufacturing variability information according to the assumed variability model below. A clock signal with 30ps transition time is given to the source of clock distribution network. Manufacturing variability of interconnects is not considered.

This analysis assumes that the variability of threshold voltage V_{th} consists of random and spatially-correlated components. The random component is size dependent [11]; the variability is significant in a small transistor and it becomes less significant as the size increases. In this analysis, we build a large driver by connecting a number of small unit drivers in parallel, because each small unit driver has an independent random value and it cancels each other in the case of building a large driver. We assumed that the spatially-correlated component has the correlation coefficient expressed as $f(x) = e^{-2x}$, where x [mm] is the distance of two devices [6]. For the small unit driver, the total standard deviation of these components is 25mV, which is considered to be appropriate in 90nm technology [6], and these variances are the same value.
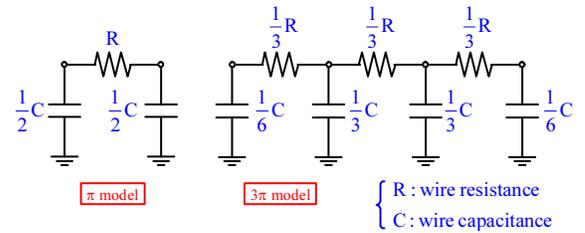

Figure 3. π **ladder model.**

FFs are not placed uniformly, and in some cases, FF densities are much different inside a chip. Even inside a functional block, the FF placement is often far from uniform distribution. This non-uniform FF placement has been a major source of clock skew so far, and we will evaluate the importance of FF placement quantitatively comparing with manufacturing variability. We used FF placement distributions of two actual designs (FPU [12] and MeP [13]), layouted by a commercial place-and-route tool with the 90nm industrial standard cell library. These FF distributions are shown in Figures 4 and 5. The numbers of FFs in FPU and MeP are 667 and 4411, respectively. The input capacitance of each FF is 1.9fF. These locations and capacitances are relatively extended for a 1mm square clock domain. To make a comparison, we also build uniform FF distributions. The FF load capacitance is uniformly distributed with a $40\mu m$ resolution. The total load capacitance is identical to those of the actual layouts. The FFs are connected to the nearest mesh segment (Figure 6).

To reveal dominant variabilities, we evaluate clock skew with various combinations of these variabilities. We also examine a tree clock distribution, in which the mesh shunts are simply removed, to confirm the effectiveness of mesh in clock skew reduction. In this case, FFs are connected to the nearest final-stage driver.
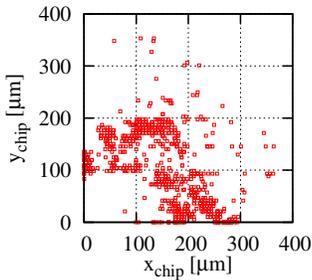

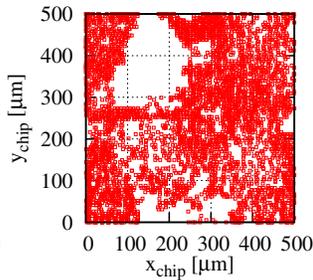**Figure 4. FF distribution (#FFs = 667, FPU).**

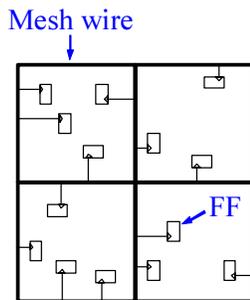**Figure 5. FF distribution (#FFs = 4411, MeP).**

Figure 6. Mesh-FF connection.

3.3. Results

Figure 7 shows the skew histogram in the case that random and spatially-correlated V_{th} variabilities and non-uniform FF placement of MeP are given. Figures 8-10 are the histograms excluding each of random V_{th}, spatially-correlated V_{th}, and FF placement variation, respectively. Table 1 lists the average and standard deviation of the maximum skew with various combinations of these variabilities.

Figures 7 and 8 are similar to each other. This indicates that the total skew is very dependent of spatially-correlated variability. On the other hand, the skew histogram in Figure 9 is very sharp, which means the skew variation due to random component is small. The skew variation is reduced by the mesh structure and the large drivers in which random variability is averaged out.

Figure 11 shows an example of V_{th} variation. At each position, there are several transistors, and then the average of them is depicted. Figure 12 shows the arrival times of the clock signal at each FF, when the variability of Figure 11 is given. We can see that the arrival times are smoothed and the peaks corresponding to V_{th} local variations are flattened. The difference of arrival time between adjacent nodes is averaged by the mesh shunt connection. On the other hand, the clock arrival time changes along with the global V_{th} gradient, which results in a large clock skew. The mesh shunt has non-negligible resistance, and hence the effective area of the averaging effect is limited. Thus, the mesh-style clock distribution is robust to random variations, and is not so tolerant to spatially-correlated variation. We therefore do not pay much attention to random variation as long as the mesh-style clock distribution, and we should focus on how to mitigate the clock skew caused by the spatially-correlated variability.

When FFs are uniformly distributed, the average of the clock skew becomes smaller (See Figures 7 and 10). However, in the case of MeP, the non-uniformity of FF placement is not severe (Figure 5), and then the skew difference in terms of FF placement is 4 to 6 ps and is not quite large (Table 1). On the other hand, in the case FPU design (Figure 4), the FFs are not well distributed, and hence the non-uniform placement increases the clock skew by over 10ps. As for the variance of the clock skew, the standard deviation is comparable regardless of the uniform and non-uniform placement both in MeP and FPU.

To clearly observe the skew reduction effect by the mesh shunt, we evaluate the clock skew for a tree-only distribution without mesh shunts. The results are also listed in Table 1. When the shuts are removed, the clock skew becomes 5 to 8 times larger, which means the shunts are very effective for designing a clock distribution with small clock skew.
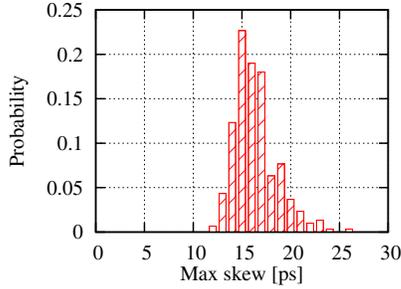
Figure 7. Skew with random and spatially-correlated V_{th} variations and non-uniform FF placement of MeP.
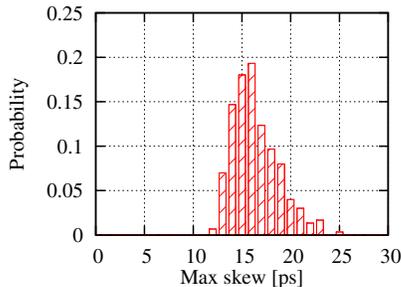

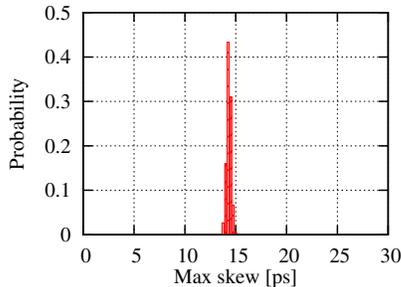**Figure 8. Skew with spatially-correlated V_{th} variation and non-uniform FF placement of MeP.**

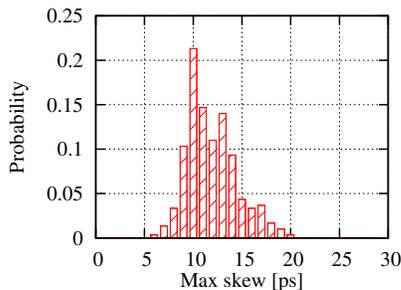**Figure 9. Skew with random V_{th} variation and non-uniform FF placement of MeP.**

Figure 10. Skew with random and spatially-correlated V_{th} variations and uniform FF placement of MeP.
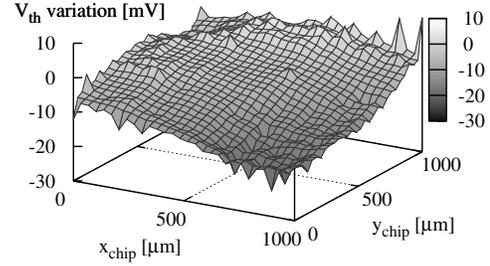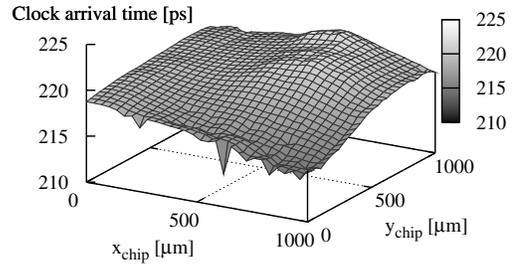

Figure 11. V_{th} variation.

Figure 12. Clock arrival time.

3.4. Skew evaluation under various mesh pitches and fanouts

In the previous subsection, the mesh pitch is fixed to 100μm and the effective fanout ($\lambda = C_{out}/C_{in}$) is set to 5. In this subsection, we regard the mesh pitch and λ as design parameters, and evaluate the clock skew varying these design parameters.

We first analyze the clock skew changing the mesh pitches from 30μm to 500μm. When changing the mesh pitch, the wire widths of the tree and the mesh are adjusted so that the total wiring area excluding the mesh-FF wires is unchanged. Although the number of branches to the final drivers in the tree varies according to the mesh pitch, the number of driver stages in the tree is fixed so as not to change the clock latency drastically.

Figure 13 shows the relation between the clock skew and the mesh pitch when the random and spatially-correlated V_{th} variabilities and non-uniform FF placement of MeP are given and λ is 5. The error bar indicates the standard deviation. As the mesh pitch becomes 150μm and above, the skew increases rapidly, because longer mesh shunt diminishes the averaging effect of clock skew reduction. On the other hand, when the mesh pitch is 150μm to 30μm, the clock skew is almost the same.

We found an interesting reason that the resistance between two nodes increases when the mesh becomes finer while keeping the total wiring area unchanged. To illustrate the fact, we compute the resistance between the corner node (In) and the node on the diagonal line (Out), as shown

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Table 1. Average μ and standard deviation σ of max skew.

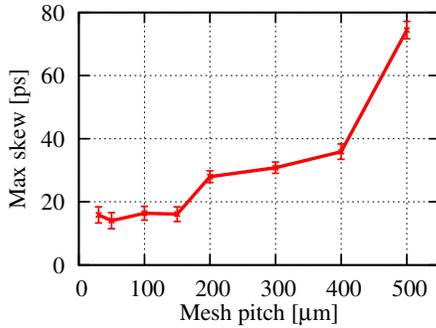| Core	Variability	$\mu \pm \sigma$ [ps]					
		non-unif. FF			unif. FF		
FPU	random, spatially-correlated	18.20	$\pm$	1.77	6.91	$\pm$	1.57
	spatially-correlated	18.39	$\pm$	1.87	6.99	$\pm$	1.69
	random	17.36	$\pm$	0.19	4.68	$\pm$	0.16
	none	17.36			4.61		
	tree-only	134.12	$\pm$	5.94	42.45	$\pm$	4.58
MeP	random, spatially-correlated	16.38	$\pm$	2.19	11.83	$\pm$	2.53
	spatially-correlated	16.39	$\pm$	2.35	12.06	$\pm$	2.56
	random	14.31	$\pm$	0.22	7.80	$\pm$	0.23
	none	14.31			7.72		
	tree-only	74.72	$\pm$	4.05	37.90	$\pm$	4.12

Figure 13. Relation between max skew and mesh pitch.

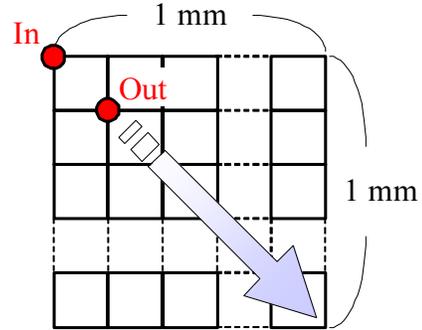**Figure 14. Calculation of R between a mesh corner node and a diagonal node.**

in Figure 14. The widths of wires in the cases of 100μm and 50μm mesh pitches are 0.64μm and 0.33μm, respectively. Figure 15 shows the resistance between In and Out, and the horizontal axis is the Manhattan distance between In and Out. Figure 16 shows the resistance increase comparing 50μm mesh pitch with 100μm mesh pitch. The resistance with 50μm mesh pitch is larger, and especially, the increasing rate is higher in the case of short distance. Therefore, the finer mesh increases the resistance between neighboring nodes, i.e. the finer mesh reduces the averaging effect of mesh shunts, which results in the increase in clock skew. We might intuitively think that the finer mesh gives better performance in clock skew reduction, but this is not true. The mesh with very fine mesh is not necessarily effective for clock skew reduction.

We secondly evaluate the clock skew varying effective fanout λ from 3 to 20. The experimental condition is similar to the previous condition, except that the mesh pitch is fixed to 100μm. Figure 17 shows the clock skew and dynamic energy per a clock cycle. The larger fanout increases the clock skew, but it reduces the dynamic energy. Figure 18 shows the latency from the source to the FFs. When the fanout varies from 3 to 20, the latency increases by over 300%. On the other hand, the clock skew increases by 50%. We think that the skew increase by weakening driver strength is limited and the robustness does not deteriorate so much thanks to the mesh shunts.

Compared to a tree-only distribution, the mesh-style distribution achieves small clock skew, and then we may have a possibility to reduce the clock energy by controlling the fanout in the case that the target skew is satisfied. When assuming the mean + sigma target clock skew is required to be below 20ps, we can choose the effective fanout λ of 7, which results in 60% dynamic energy reduction compared to λ=3.

4. Conclusion

We evaluated clock skew considering manufacturing variability of $\mathtt{Vth}$ and FF placement in mesh-style clock
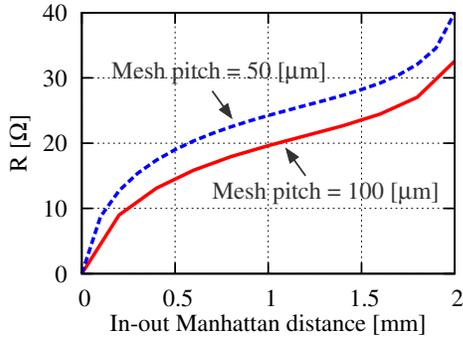
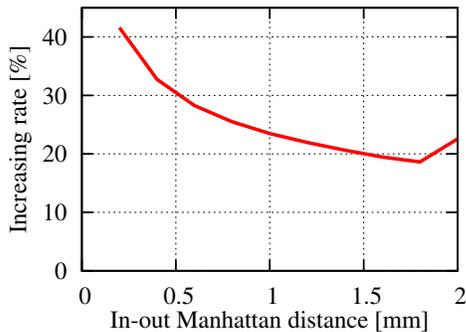**Figure 15. Resistance between mesh nodes.**

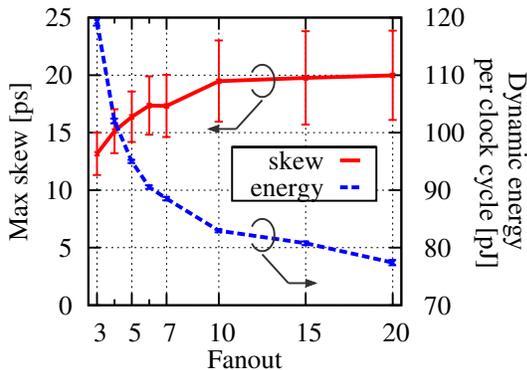**Figure 16. Increasing rate of resistance.**

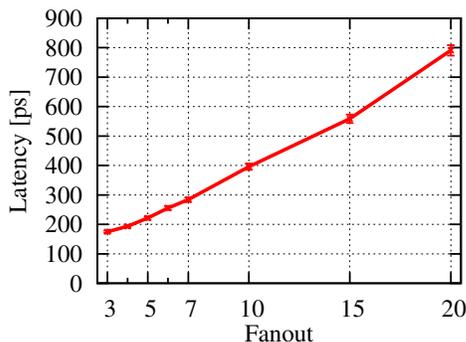**Figure 17. Max skew and dynamic energy vs. fanout.**

Figure 18. Latency vs. fanout.

distribution in a 90nm technology. The spatially-correlated variation has more impact on clock skew than random variation. Non-uniformity of FF placement can be a large source of clock skew. We revealed that the finer mesh is not necessarily effective for clock skew reduction, because of resistance increase between neighboring nodes. We also discussed the possibility that clock mesh is suitable for low energy clock distribution by controlling the driver fanout.

5. Acknowledgement

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