Statistical Timing Analysis Considering Spatially and Temporally Correlated Dynamic Power Supply Noise

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ABSTRACT

Power supply noise is becoming more and more influential on timing, though noise aware timing analysis has not been well established yet, because of several difficulties such as its dependency on input vectors and dynamic behavior. This paper proposes a static timing analysis considering power supply noise in which the dependency of noise on input vectors and spatial and temporal correlations are handled in a statistical manner. We construct a statistical model of power supply voltage that dynamically varies with spatial and temporal correlation, and represent it as a set of uncorrelated variables. We demonstrate that power voltage variation is highly correlated and adopting principal component analysis as an orthogonalization technique is effective in variable reduction. Experiments confirm the validity of our model and the accuracy of timing analysis. We also discuss the accuracy and CPU time in association with variable reduction.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids—*Simulation*

General Terms

Design, Experimentation, Verification

Keywords

Statistical timing analysis, Power supply noise, Principal component analysis, Gaussianization

1. INTRODUCTION

In nano-meter technology era, manufacturing variability fluctuates circuit performance significantly, and variation-aware timing analysis has been intensively studied[1, 2, 3]. In addition, timing verification considering power/ground noise has been eagerly demanded. Power supply noise is expected to become a more and more serious problem on timing in the future because of increasing current consumption and decreased power supply voltage. A severe obstacle for noise aware timing analysis is the difficulty to identify the worst-case noise for timing. Power supply noise depends on given input signals and internal register states, and changes within a clock cycle as well as cycle by cycle. As circuit scale becomes larger, the combinations of input signals and register states increase exponentially, which makes it prohibitively expensive to find the true worst-case noise.

Dynamic timing simulation with power/ground network and input patterns can provide timing information with noise. However, dynamic timing analysis can not cover all paths, and verifies part of path delays, which is a well known drawback. Even if a test pattern that maximizes voltage drop is found, the vector does not necessarily correspond to the worst-case for timing, because the circuit structure and the layout are also associated with the timing. Preparing effective test vectors for noise aware dynamic timing verification is a computationally expensive problem, and it is impossible to solve in a practical time.

To consider the impact of power/ground noise on timing, static timing analysis (STA) is commonly performed supposing that a constant (DC) voltage drop, for example the maximum voltage variation, is given to all gates. This approach is computationally efficient, but there is no systematic way to determine the voltage drop without optimism and excessive pessimism. When the maximum voltage drop is given to all gates, the estimated timing is too pessimistic, which causes timing convergence problem and overdesign. To solve this problem, timing analysis considering dynamic voltage variation has been proposed[4, 5], and some commercial tools are available. However, it is necessary to obtain or assume the worst-case noise, which means the pattern-dependency problem of power supply noise remains unsolved.

Although finding the exact worst-case noise for timing is extremely difficult, designers have to assure that the designed circuit operates at the target frequency in a quantitative manner before fabrication. Therefore, a systematic technique that can estimate not exact but reasonable worst-case timing is necessary. Path-based methods to estimate the maximum delay have been proposed[6, 7, 8]. These methods, however, have to be applied to many potential critical paths, and hence the computational cost could be very high. Recently, Ref. [9] has proposed an approach to estimate the effect of power supply noise on timing by solving an optimization problem. The problem is formulated as a non-linear delay maximization problem under the given constraints of current consumption. However, the circuit size reported in [9] is limited, and the applicability to larger circuits is not clear. As another approach, a statistical treatment has been introduced into power supply noise aware timing analysis[10, 11, 12]. Reference [10] estimates voltage variation by convolution of statistically modeled current consumption and impulse response of power/ground network. In [11], first, authors derive the average and the standard deviation of every block and

ISPD'08, April 13–16, 2008, Portland, Oregon, USA.

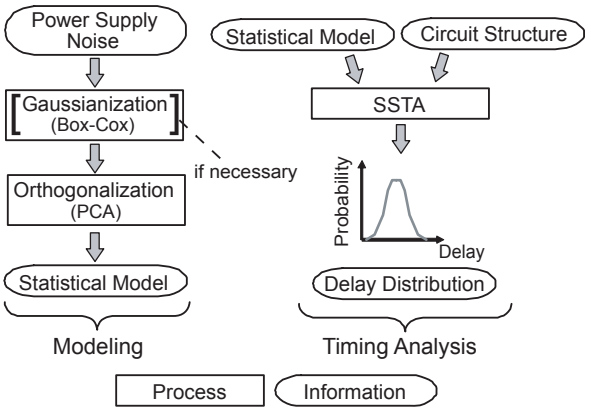

Figure 1: Overall view of proposed approach.

the correlation coefficients between blocks, and then estimate the delay. Reference [12] focuses on spatial correlation of power supply noise and proposes to use principal component analysis (PCA) for modeling of power supply noise. Path delay distribution is then computed with uncorrelated variables. We know an argument that timing failure due to power supply noise must be verified in a deterministic manner, since a certain input pattern necessarily causes a problem. However, an exact verification in a vast input pattern and register state space is impossible, and thus we believe that a statistical approach helps designers estimate timing performance quantitatively and systematically.

In this paper, we propose a statistical timing analysis method considering dynamic power supply noise. The overall flow of the proposed method is shown in Fig. 1. The proposed method models power/ground noise statistically. Spatially and temporally correlated power supply noise is transformed to uncorrelated variables by using orthogonalization techniques, such as PCA and independent component analysis (ICA). We then perform statistical static timing analysis using the derived statistical power/ground noise model. Statistical timing analysis with a statistical model of power supply noise with PCA has been proposed by Kim[12], however, it is a preliminary work and several important issues, such as non-Gaussian distribution shape of variables and dynamic voltage fluctuation within a clock cycle, remain unsolved or not addressed. Further, variable reduction by PCA due to tight correlation among variables is not aggressively exploited for reducing CPU cost of statistical timing analysis.

In this work, we experimentally demonstrate that PCA-based statistical modeling, with some distribution transformation techniques (e.g. Box-Cox transformation) if necessary, works well, though the distribution of power supply noise is not exactly Gaussian. To take dynamic noise behavior within a clock cycle into consideration, we propose to discretize a clock cycle into several time slots, and assign a random variable to each time slot to construct a statistical model of dynamic power supply noise. We focus on an observation that power supply noise is highly correlated not only spatially but also temporally, and model power supply noise with a small set of random variables, which helps to reduce CPU time for timing verification. We also demonstrate that adaptive spatial discretization for variable assignment reduces PCA cost significantly. You might think that SSTA with PCA is a well-known approach, but this similarity is a big advantage to keep the compatibility to conventional SSTA, and the proposed method can be easily integrated into SSTA tools for manufacturing variability, i.e. statistical timing analysis considering both manufacturing variability and power supply noise is easily realized in a unified approach.

This paper assumes that information on power supply noise needed for the statistical modeling is given. Generally, the estimation of power supply noise is not easy. We, however, think that sophisticated methods, such as impulse response and convolution with logic simulation results for power estimation and functional verification[9] give us the information. An efficient information preparation is another research topic to study, and hence we do not discuss it further in this paper.

This paper is organized as follows. Section 2 discusses difficulties of timing analysis considering power supply noise. We show how to statistically model power/ground voltage variation in Section 3 . Section 4 explains SSTA procedure with the proposed noise model. We demonstrate experimental results in Section 5, and Section 6 concludes the discussion.

2. DIFFICULTIES OF NOISE AWARE TIMING ANALYSIS AND PROPOSED APPROACH

When performing timing analysis considering power supply noise, a problem is that the maximum voltage drop does not necessarily cause the worst-case delay. The supply voltage changes spatially and temporally within a clock cycle as well as cycle by cycle. The observation of power supply noise only can not necessarily detect a timing failure due to power supply noise, because the timing depends on the position of critical paths as mentioned in [9].

Figure 2 shows an example that the maximum voltage drop does not always cause the worst delay. The solid lines and broken lines represent power supply noise of cycle #(c) and cycle #(d) respectively. Suppose a critical path exists in area A. In this case, the delay of cycle #(c) would be worse than that of cycle #(d). However, if a critical path is located in area B, it is unclear which cycle is the worse-case for timing in this chip. In area B, the noise of cycle #(c) delays the gate switching at the beginning of clock cycle, whereas it less affects the switching at the latter half of clock cycle. On the other hand, in cycle #(d), the switching at the latter half is much slowed down. Thus, the voltage fluctuation within a clock cycle can influence the gate delay much or less depending on the switching timing, where the switching timing is basically determined by the circuit structure.

The noise waveform shape varies according to given input vectors. As mentioned earlier, the space in input vectors and internal logic states is tremendously huge and can not be explored thoroughly. We thus model power supply noise statistically preserving the spatial and temporal correlation, and apply it to a statistical static timing analysis. The proposed approach can solve the problem described above, i.e. the position of critical paths and spatial and temporal difference of power supply noise are considered simultaneously. We report an experimental result that the maximum noise does not necessarily involve the worst-case delay in Section 5.

Principal component analysis (PCA), which is one of orthogonalization methods, has a preferable advantage. Highly correlated Gaussian variables are transformed into a small set of Gaussian variables with a small sacrifice of accuracy. We here show an example that power supply noise is highly correlated in space. We evaluated power supply noise of an FPU circuit in $1\times1\text{mm}^2$ area[13], and set 10×10 variables associated with spatially divided 10×10 grids. Each variable represents cycle-average supply voltage of

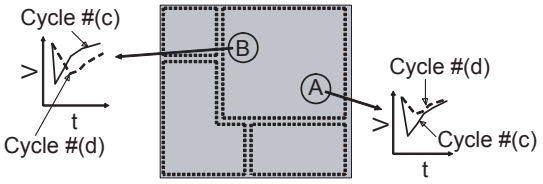

Figure 2: Different waveforms of power supply noise in space and time.

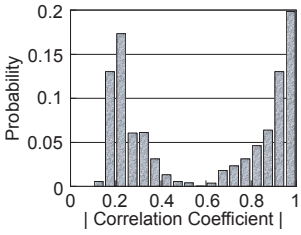

Figure 3: Spatial correlation of power supply voltage.

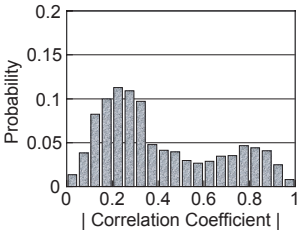

Figure 4: Spatial correlation of current consumption.

$V_{\rm DD}$ side at each grid. The evaluation condition is the same with experiments in Section 4. Figure 3 shows the histogram of correlation coefficients between variables. We can see that variables are highly correlated, and 36.2% of coefficients are above 0.9 indeed. We thus expect that a compact statistical model with a small number of variables is derived. A small number of variables enable us to perform SSTA and Monte Carlo simulation efficiently. On the other hand, when we choose current consumption as a variable instead of supply voltage, the correlation between the variables is weaker than power supply voltage as shown in Fig. 4, and hence variable reduction can not be efficient. Although current consumptions at the adjacent nodes are not much correlated, the impedance of the power network strengthens the spatial correlation of power supply voltage.

When using PCA, we have to pay attention to the distribution shape of variables, because PCA assumes Gaussian distribution. A problem to apply PCA to power supply noise modeling is non-Gaussian noise distribution, which may cause undesirable modeling error. Solutions to this problem include Gaussianizing the variables, e.g. Box-Cox transformation[14]. This transformation improves Gaussianity of the variable. In this paper, we experimentally demonstrate that PCA-based modeling is reasonable from the standpoint of practical use, though, rigidly speaking, the distribution is not Gaussian. When the variables are quite far from Gaussian distribution, another orthogonalization technique, such as independent component analysis, should be applied, which is similar to [3].

An advantage of the proposed method using variable orthogonalization is a compatibility with SSTA developed for manufacturing variability[1, 2, 3]. The derived statistical model of power supply noise is expressed in a similar manner with manufacturing variability, and thus importing noise effect to SSTA is straightforward, though handling within-cycle voltage variation requires a modification. We therefore can perform SSTA covering both the process and voltage variation in a unified manner. The proposed method has a possibility to give a new sign-off criteria that considers both manufacturing and voltage variation, though there remains several points to study.

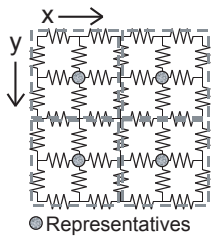

Figure 5: Spatial discretization. Divided into partitions with broken lines.

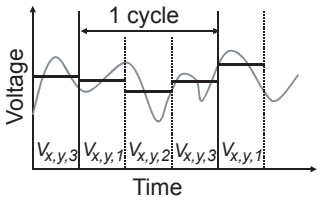

Figure 6: Temporal discretization. Dividing a clock cycle into time spans.

3. PROPOSED STATISTICAL MODELING OF POWER SUPPLY NOISE

This section explains the proposed modeling of power supply noise. From now, we assume distributions of power supply voltage are Gaussian or can be transformed to Gaussian by variable transformation techniques. We thus use PCA as an orthogonalization method in this paper. We experimentally demonstrate non-Gaussianity of the distribution is not significant in Section 5. Note that even when distribution of power supply noise is far from Gaussian, the basic concept of the proposed method works by using ICA instead of PCA similar to [3].

3.1 Spatial and temporal discretization

Power supply noise varies continuously in space and time, and rigidly speaking, every cell has different noise waveform. However, observation points of power supply noise are limited because of cost, and the number of points is much reduced by clustering cells. We first set up observation points by discretizing a chip spatially. We also discretize power supply variation within a clock cycle temporally. We then assign a random variable to each time span at each spatial grid.

Spatial discretization is performed by partitioning a chip/block area into a 2D grid and choosing a representative value for each divided partition. As a representative value, for example, the voltage at the center point (Fig. 5) or the average voltage in each partition is a candidate. The voltages of all nodes in the same partition are assumed to be identical.

Figure 5 is an example of uniform discretization, which is widely used for manufacturing variability modeling. In the case of power supply noise, more sophisticated discretization is desirable, since power/ground voltage sometimes fluctuates locally. Fine discretization should be applied to heavily fluctuating area, whereas coarse discretization is good enough for calm area. We here explain an adaptive discretization method as an example. First, we divide a chip/block area into partitions which include only a single observation node. We then assess whether two partitions can be regarded to have the same voltage fluctuation, i.e. the differences of average and standard deviation are small enough and the correlation coefficient is large enough. When these partitions can be regarded as equivalence, we merge these partitions into a single partition. This operation continues until all primal partitions are evaluated.

Another important difference of power supply noise from manufacturing variability is its dynamic behavior. Temporal continuousness also needs to be removed. We partition a clock cycle into several time spans, and compute a representative voltage (e.g. average as shown in Fig. 6).

We then treat the value at every clock cycle as a different sample. Figure 6 shows an example when the voltage at position (x, y)

is divided into three time spans and its random variables are denoted as $V_{x,y,1}$, $V_{x,y,2}$ and $V_{x,y,3}$. The number of time spans is determined according to the modeling requirement, i.e. when we need to accurately model dynamic variation within a clock cycle, the number of spans should be increased, otherwise a few spans are sufficient.

3.2 Variable transformation with orthogonalization

Given a set of variables, we translate the variables and derive a compact statistical model with Gaussianization and orthogonalization.

3.2.1 Gaussianization

The first step of the variable transformation is to improve Gaussianity of the variables. This step can be skipped when the supply voltage distribution can be reasonably treated as Gaussian. A famous transformation to improve Gaussianity is Box-Cox transformation[14]. There are several transformation equations of Box-Cox transformation, and the equation we use in this paper is expressed as follows.

$$\hat{z} = \begin{cases} \frac{z^{\Lambda}-1}{\Lambda} & (\Lambda \neq 0), \\ \log(z) & (\Lambda = 0), \end{cases} \tag{1}$$

where z is the original variable, $\hat{z}$ is the transformed variable and Λ is a parameter. In our modeling, z corresponds to a variable of power supply noise $V_{x,y,t}$. The optimum Λ that maximizes Gaussianity is computed for every variable $V_{x,y,t}$ individually by maximum likelihood procedure, and is given to SSTA.

3.2.2 Orthogonalization by PCA

PCA maps a given set of correlated random variables to a new set of uncorrelated random variables, which are called principal components (PCs). Given a variance-covariance matrix, PCA transforms the variable z_i into Eq. (2), where λ_j is the jth largest eigenvalue, e_{ij} is the element of the jth eigenvector which corresponds to z_i, μ_i is the average of z_i, and σ_i is the standard deviation of z_i. k is the number of PCs and pc_j is the jth principal component. Principal component pc_j is expressed as Eq. (4), which is a linear summation of n original variables of z_i. The principal components are random variables mutually uncorrelated with each other, which eases computation of correlation significantly in SSTA[1]. Moreover, z_i is often approximated as Eq. (3) with the reduced number of PCs $k'(k' < k)$, when the original variables of z_i are correlated. When Box-Cox transformation is applied to z_i beforehand, we just replace z_i with $\hat{z}_i$ in Eqs. (2), (3) and (4).

$$z_i = \mu_i + \left(\sum_{j=1}^{k} \sqrt{\lambda_j} e_{ij} pc_j \right) \sigma_i \tag{2}$$

$$\approx \mu_i + \left(\sum_{j=1}^{k'} \sqrt{\lambda_j} e_{ij} pc_j \right) \sigma_i, \tag{3}$$

$$pc_j = \frac{1}{\sqrt{\lambda_j}} \sum_{i=1}^{n} \left(e_{ij} \frac{z_i - \mu_i}{\sigma_i} \right). \tag{4}$$

3.2.3 Computational complexity

Let m and n denote the number of samples and variables respectively. The optimal Λ for Box-Cox transformation in Eq. (1) is derived by likelihood function, and its complexity is $O(m)$. The transformation of all n variables requires the effort of $O(mn)$. On the other hand, the complexity of PCA is $O(n^3)$[1]. Consequently, the total cost of the variable transformation is $O(n^3)$. The complexity is not low, but the variable transformation is performed only once before SSTA, and hence this computational cost is expected to be acceptable, which is similar to other SSTA methods[1, 2].

Table 1: Computational time of PCA.

#variables	CPU time(s)
100	0.01
900	5.41
2500	91.3
4900	788
10000	7460

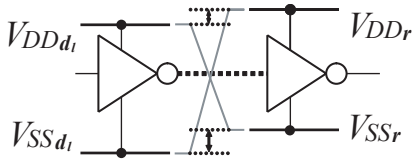

Figure 7: Power and ground level difference between a driver and a receiver.

Table 1 shows the execution time of PCA implemented in R[15] on a computer with Opteron processor 2.4GHz and 16GB memory. Even in the case that PCA cost is not acceptable, for example, the number of variables is larger than 10k, the modeling chip region can be reasonably reduced, because power voltage variation has a property of locality[16].

4. SSTA WITH STATISTICAL MODEL OF POWER SUPPLY NOISE

This section discusses the application of the statistical model of power supply noise to SSTA. The proposed model is applicable to both path-based and block-based SSTA.

Equation (5) is a common gate delay model in a canonical form that is widely used in SSTA implementation. We adopt this form, because this form realizes fundamental sum and max operations in SSTA efficiently as long as the variables are Gaussian[1].

$$d_i = \mu_i + \sum_{j=1}^{k'} a_{i,j} pc_j. \tag{5}$$

Here, $a_{i,j}$ is a sensitivity coefficient associated with pc_j.

The power and ground level difference between drivers and a receiver affects the switching delay of the receiver, as reported in references (e.g. [9, 17]). Figure 7 explains the level difference between a driver and a receiver. Suppose the receiver is placed at (x, y) grid and switching in (t) time span. Similarly, the driver is placed at (x_l, y_l) grid and switching in (t_l) time span. $V_{\mathrm{DD}r}$/$V_{\mathrm{SS}r}$ is the supply/ground voltage of the receiver side at (x, y) grid in (t) time span. Similarly, $V_{\mathrm{DD}d_l}$/$V_{\mathrm{SS}d_l}$ is the supply/ground voltage of the lth driver side at (x_l, y_l) grid in (t_l) time span. To consider the level difference, we use the following canonical delay form.

$$d_r = \mu_r + \sum_{j=1}^{k'} \sqrt{\lambda_j} A_{r,j} pc_j, \quad (6)$$

$$A_{r,j} = \sigma_{V_{\mathrm{DD}r}} \frac{\partial d_r}{\partial V_{\mathrm{DD}r}} e_{(V_{\mathrm{DD}r}),j} + \sigma_{V_{\mathrm{SS}r}} \frac{\partial d_r}{\partial V_{\mathrm{SS}r}} e_{(V_{\mathrm{SS}r}),j} + \sum_l \left(\sigma_{V_{\mathrm{DD}d_l}} \frac{\partial d_r}{\partial V_{\mathrm{DD}d_l}} e_{\left(V_{\mathrm{DD}d_l}\right),j} + \sigma_{V_{\mathrm{SS}d_l}} \frac{\partial d_r}{\partial V_{\mathrm{SS}d_l}} e_{\left(V_{\mathrm{SS}d_l}\right),j} \right). \quad (7)$$

The first and second terms in RHS of Eq. (7) correspond to the delay variation due to the voltage variation at the receiver. The other terms mean the delay variation caused by the voltage variation at the driver. In multiple-input cells, there are several inputs. Even the voltages of stable (not switching) inputs affect the propagation delay[17], and hence we sum up the terms with respect to every voltage variable at drivers.

When the Box-Cox transformation is applied, V_{DD} and V_{SS} are translated into $\hat{V}_{\mathrm{DD}}$ and $\hat{V}_{\mathrm{SS}}$. $\partial d/\partial \hat{V}$ is the sensitivity of the delay to $\hat{V}$, and is easily computed from $\partial d/\partial V$ and the derivative of Eq. (1). The form of Eq. (6) is compatible with Eq. (5), and hence we can easily take manufacturing variability and power supply noise into consideration in the same manner.

Unlike the process variation, the proposed method needs a special consideration. In the case of spatial discretization, a grid, i.e. a variable parameter, is assigned to a gate definitely. However, in the case of temporal discretization, the correspondence to a variable is sometimes obscure, because a switching transition may occur at the boundary of temporal division. Furthermore, when the temporal division is rough, i.e. the number of time span is small, the voltage difference between successive two time spans is large, which may cause a large timing estimation error near the boundary. In order to mitigate this error, we revise a weighted-average calculation to cope with a case that input and output transition timings of a gate are included in different time spans. Let t_I and t_O represent input and output transition timings, where each time belongs to Span #(m) and Span #($m+1$) respectively. First, we estimate t_O with the use of μ_{r_m} which is the average delay in Span #(m), that is t_O = t_I + μ_{r_m}. Using these values, average μ'_r and the coefficient of Eq. (6), $a'_{r,j}$, are recalculated by

$$\mu'_r = \frac{\Delta t_I}{\Delta t_I + \Delta t_O} \mu_{r_m} + \frac{\Delta t_O}{\Delta t_I + \Delta t_O} \mu_{r_{m+1}}, \quad (8)$$

$$a'_{r,j} = \frac{\Delta t_I}{\Delta t_O + \Delta t_O} a_{r_m,j} + \frac{\Delta t_O}{\Delta t_I + \Delta t_O} a_{r_{m+1},j}, \quad (9)$$

where Δt_I is the time from t_I to the boundary time, Δt_O is the time from the boundary time to t_O, $\mu_{r_{m+1}}$ is the average delay of Span #($m+1$), $a_{r_m,j}$ and $a_{r_{m+1},j}$ are the coefficients of Eq. (6) in Span #(m) and Span #($m+1$), respectively.

5. EXPERIMENTAL RESULTS

This section demonstrates experimental results. We first validate the statistical modeling of power supply noise, and then verify the accuracy of the proposed timing analysis.

5.1 Experimental conditions

For constructing the proposed model of power supply noise, we use an FPU circuit and a tiny64 processor[13], as noise generators. These circuits were synthesized by a commercial logic synthesizer and placed and routed by a commercial tool with a 90nm standard cell library. The circuit sizes are 39k and 20k gates respectively. We attached a power/ground network shown in Fig. 8 to each noise generator circuit and simulated the power supply noise. A flip chip package with bump connections is assumed. Input vectors of 2000 clock cycles are given to each circuit. The simulation results are used for PCA including correlation matrix calculation. Please note that other methods for power noise estimation can be used, though a fast circuit simulator is used in this paper.

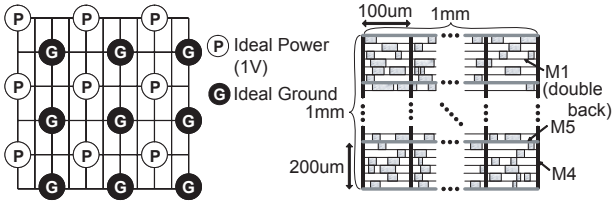

Figure 8: Power network of test circuit.

We implement block-based SSTA and Monte Carlo simulation in C++ and perform them for ISCAS85 benchmark circuits, a 64-bit multiplier, an ALU circuit for vector operation and an H-tree for clock distribution on a computer with Opteron processor 2.4GHz and 16GB memory. These circuits except H-tree were synthesized, placed and routed by commercial tools. In the H-tree, a single path is selected and its jitter is evaluated. The power supply noise of the FPU circuit or the tiny64 processor described above is given to the benchmark circuits.

5.2 Validation of statistical modeling of power supply noise

5.2.1 *Distribution of power supply noise*

We here show a distribution of power supply voltage as an example. We choose a distribution of power supply noise that is relatively far from Gaussian (Fig. 9), whereas a large portion of variables are close to Gaussian. Figure 10 is the normal probability plot of Fig. 9. In the case of a normal distribution, all dots are placed on the diagonal line. When the dots are far from the diagonal line, the distribution is much different from Gaussian. In Fig. 10, many dots are not on the diagonal line, which means the distribution is different from Gaussian, as shown in Fig. 9.

On the other hand, the variable transformed by Box-Cox transformation approaches Gaussian (Fig. 11). In the normal probability plot of Fig. 12, the dots are closely placed to the diagonal line, which means the Gaussianity is much improved. We experimentally reveal that SSTA results are accurate compared with Monte Carlo analysis, which will be discussed later in Section 5.3. We thus conclude that orthogonalization with PCA for power supply noise is reasonable.

5.2.2 *Variable reduction rate*

When the correlation between random variables is high, the original distribution can be reproduced with a small number of PCs. This section discusses how many PCs can be reduced. When we reduce the number of PCs, a metric called cumulative proportion is used[18]. The cumulative proportion is expressed as

$$cumulative\ proportion_{k'} = \frac{1}{n} \sum_{j=1}^{k'} \lambda_j, \quad (10)$$

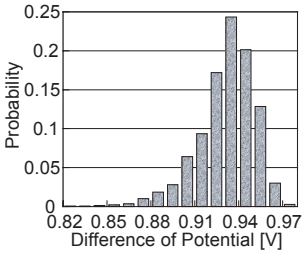

Figure 9: Supply voltage distribution before Box-Cox transformation.

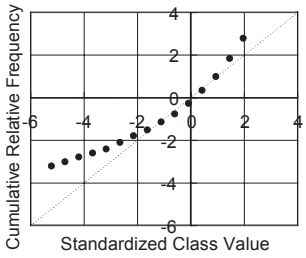

Figure 10: Normal probability plot of Fig. 9.

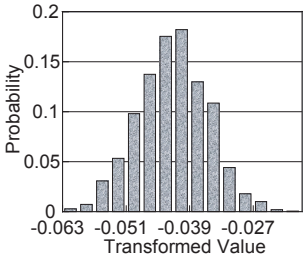

Figure 11: Distribution after Box-Cox transformation corresponding to Fig. 9.

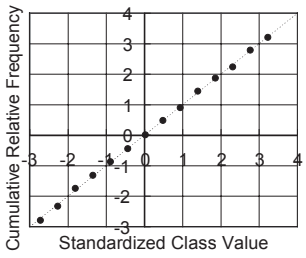

Figure 12: Normal probability plot of Fig. 11.

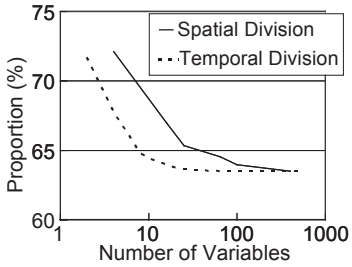

Figure 13: Proportion of the first principal component.

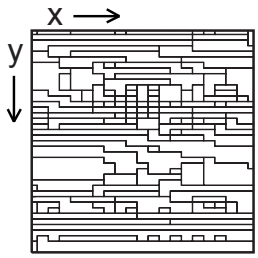

Figure 14: Adaptive spatial discretization.

where n is the number of the variables. As the cumulative proportion approaches 1, the original distribution is well reproduced.

Figure 13 shows the proportion of the first PC (i.e. cumulative proportion$_1$) when the division number is changed. The solid line shows the relationship between the spatial division number and the proportion of variance in the case that the temporal division within a cycle is not executed. The strongly-correlated variables allow the first PC to keep high proportion. On the other hand, the broken line gives the result when the temporal division number varies while keeping the spatial division unchanged. The increase of temporal division number does not affect the proportion very much, because the parasitic capacitor in the chip smooths power supply noise and strengthens temporal correlation. Furthermore, if intentional decoupling capacitance is inserted, the spatial and temporal correlation of power supply noise becomes strong, and the modeling efficiency improves further. Power noise also has correlation with ground noise. Therefore, even when the number of variables is very large, a small number of PCs can achieve high cumulative proportion. Let us show an example. Suppose the spatial and temporal division number of the difference between power and ground are 10×10 and 10 respectively. We examine the number of PCs whose cumulative proportion exceeds 90%. Only six PCs are capable of attaining the target value, though the total number of variables is 1000. In this instance, more than 99% of the variables are reducible, which helps to reduce computational cost of SSTA, because the complexity is proportional to the number of principal components[1].

5.2.3 Adaptive spatial discretization

We show an example that the adaptive spatial discretization explained in Section 3.1 is applied to FPU. In this experiment, threshold values of average and standard deviation used for the equivalent partition checking are set to a tithe of differences between the maximum and the minimum values in the whole area, and the threshold of correlation coefficient is set to 0.9.

Figure 14 shows the result of the adaptive discretization. In this case the number of divided area is 142. The region where voltage is fluctuating locally is discretized finely. If all the area is divided with the finest resolution, the division number becomes 840. As mentioned in Section 3.2.3, the complexity of PCA is $O(n^3)$, and hence the variable reduction from 840 to 142 corresponds to up to over 200x cost reduction of PCA.

5.3 SSTA results for power supply noise

We first verify the accuracy of the proposed timing analysis method. In this experiment, the numbers of spatial and temporal division are set to 10×10 and 10, respectively. Here, we perform Monte Carlo by using the noise information of 2000 cycles that is the same with the information given to PCA. Noisy power voltage waveforms of each cycle is are given for all cells considering the placement. The delay of each cell is calculated with the voltage value corresponding to the cell position and switching timing. With these gate delays, conventional STA is performed and the circuit delay of each cycle is obtained. Therefore, the number of Monte Carlo evaluation is 2000. The Monte Carlo result does not include the errors that originate from discretization, PCA for incomplete Gaussian distribution and SSTA operation. The results of Monte Carlo are compared to those of SSTA as ideal solutions.

Table 2 lists the average and standard deviation of the delay acquired by SSTA with and without Box-Cox transformation and Monte Carlo simulation. We can see that the proposed SSTA with and without Box-Cox transformation estimates the timing accurately. The estimation error of the average delay is 0.465% and that of the standard deviation is 14.4%. The accuracy improvement due to Box-Cox transformation is not significant, but it reduces the estimation error of standard deviation from 14.4% to 12.7%. The effect of Box-Cox transformation is limited, because most variables are originally close to Gaussian. When the noise information of tiny64 processor is given, the errors of average and standard deviation are 0.566% and 19.7% respectively. The proposed method

Table 2: Accuracy of timing estimation (FPU).

circuit	# cells	SSTA w/o Box-Cox trans.		SSTA w/o - MC		SSTA w/ Box-Cox trans.		SSTA w/ - MC		Monte Carlo (MC)		delay w/o noise
		avg (ps)	sd (ps)	avg (%)	sd (%)	avg (ps)	sd (ps)	avg (%)	sd (%)	avg (ps)	sd (ps)	(ps)
c432	232	843.1	11.1	0.522	7.58	842.7	10.8	0.478	4.21	838.7	10.4	716.1
c1355	329	477.8	4.98	1.32	28.2	477.6	4.90	1.27	29.4	471.6	6.94	399.7
c1908	387	737.7	15.0	0.548	27.3	737.1	14.6	0.472	24.1	733.6	11.8	619.3
c6288	3382	2755	35.3	0.331	10.3	2754	34.9	0.370	9.15	2764	32.0	2371
c7552	2070	725.7	13.6	0.121	17.5	725.4	13.2	0.172	13.8	726.6	11.6	608.9
multiplier	41629	1839	19.9	0.102	8.45	1839	19.7	0.0969	7.23	1837	18.3	1590
ALU	14655	1075	12.3	0.192	3.79	1075	12.2	0.216	2.87	1077	11.8	907.0
H-tree	7	194.2	1.53	0.584	11.8	194.2	1.52	0.576	10.8	193.0	1.37	171.7
average	-	-	-	0.465	14.4	-	-	0.456	12.7	-	-	-

Table 3: Accuracy and #PCs (multiplier, tiny64).

#PCs	c.prop.(%)	avg(ps)	sd(ps)	CPU time(ms)
1	84.2	1843	0.384	164
2	92.9	1843	3.16	166
4	95.8	1843	3.71	180
8	98.4	1843	4.07	205
16	99.5	1843	4.09	238
2000	100	1843	4.09	11800

helps designers to quantitatively know how the circuit delay fluctuates depending on input vectors in a systematic way.

The Monte Carlo results show the worst-case delay does not always occur when power/ground noise is maximum. In circuit c1355, even when the supply voltage, which is averaged temporally within a clock cycle and spatially within a block area, is the minimum, the circuit delay is not the largest. This situation indeed corresponds to the case of the 970th longest circuit delay among 2000 evaluated cycles. Thus, finding the maximum power/ground noise is not sufficient for timing verification.

Table 3 shows the relation between the number of PCs (cumulative proportion) and delay estimation accuracy for 64-bit multiplier. The spatial and temporal division number are 10×10 and 10 respectively and the noise generator is tiny64 processor. In this case, the result with only eight PCs is very close to that with all PCs, which enables considerable variable reduction. The CPU time is reduced from 11800ms to 205ms by 98.3%.

5.4 SSTA result both for power supply noise and manufacturing variability

We finally demonstrate that the proposed method estimates delay distribution considering both dynamic power supply noise and static manufacturing variability in a unified manner. In this experiment, threshold voltage (Vth) is fluctuated. Its variation consists of a spatially correlated constituent and a random fluctuation constituent. As for the spatial correlation, we assume that the correlation coefficient of Vth is given by a function $f(x) = e^{-2x}$, where $x$mm is the distance between two gates[19]. We suppose that the magnitudes of both variational components are the same and the total standard deviation is 25mV, which is a typical value in a 90nm process[19]. For the sake of simplicity, intra-gate fluctuation is not considered in this experiment. We also assume that manufacturing variability and power supply noise are uncorrelated in this experiment, though this mutual dependence is analyzed in [20]. The mutual correlation can be modeled by PCA in nature, as long as we can obtain the statistical data. Here, this experiment aims to

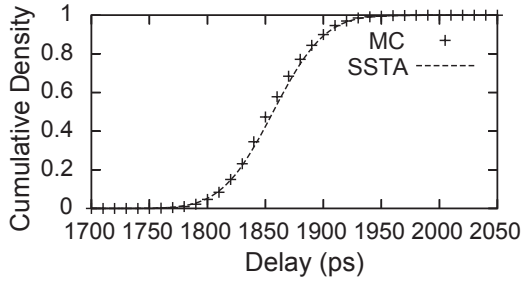

Figure 15: CDF of delay distribution considering process and power supply fluctuation.

demonstrate the feasibility that the proposed method can cope with manufacturing variability and power supply noise in a unified approach.

Figure 15 shows the delay distribution of a 64-bit multiplier in the case that the spatial and temporal division numbers are set 10×10 and 10 respectively. The power supply noise of FPU is given. The difference of two distributions at 50% cumulative density is 4ps, and it is a quite small error, which means the proposed method well copes with both variabilities. If the timing margin 3σ is set for each variation individually, total margin becomes 142.7ps. However, simultaneous consideration of the variations by the proposed method reduces timing margin to 104.8ps. This result indicates a possibility that the proposed method gives a new sign-off criteria both considering manufacturing and supply voltage fluctuation, though several studies are needed before applying it to a practical design.

6. CONCLUSION

In this paper, we proposed SSTA considering dynamic power supply noise with orthogonalization technique. We confirmed that dynamic power/ground noise could be modeled statistically with PCA though the distribution of power supply voltage was not rigidly Gaussian. The experiments showed that the proposed method estimated delay variation due to power supply noise accurately. We experimentally demonstrated that a small number of principal components obtained by PCA were capable of accurate delay estimation thanks to spatial and temporal correlation of power supply noise.

7. ACKNOWLEDGEMENT

This work is supported in part by Semiconductor Technology Academic Research Center (STARC), New Energy and Industrial

Technology Development Organization (NEDO) and VLSI Design and Education Center (VDEC).

8. REFERENCES

[1] H. Chang and S. Sapatnekar, "Statistical Timing Analysis under Spatial Correlations," *IEEE Trans. CAD*, Vol. 24, No. 9, pp. 1467–1482, 2005.

[2] C. Visweswariah, K. Ravindran, K. Kalafala, S. G. Walker, and S. Narayan, "First-order Incremental Block-Based Statistical Timing Analysis," in *Proc. DAC*, pp. 331–336, 2004.

[3] J. Singh and S. Sapatnekar, "Statistical Timing Analysis with Correlated Non-Gaussian Parameters using Independent Component Analysis," in *Proc. DAC*, pp. 155–160, 2006.

[4] K. Shimazaki, M. Fukazawa, M. Nagata, S. Miyahara, M. Hirata, K. Sato, and H. Tsujikawa, "An Integrated Timing and Dynamic Supply Noise Verification for Nano-meter CMOS SoC Designs," in *Proc. CICC*, pp. 31–34, 2005.

[5] M. Hashimoto, J. Yamaguchi, T. Sato, and H. Onodera, "Timing Analysis Considering Temporal Supply Voltage Fluctuation," in *Proc. ASP-DAC*, pp. 1098–1101, 2005.

[6] J.-J. Liou, A. Krstic, Y.-M. Jiang, and K.-T. Cheng, "Path Selection and Pattern Generation for Dynamic Timing Analysis Considering Power Supply Noise Effects," in *Proc. ICCAD*, pp. 493–496, 2000.

[7] G. Bai, S. Bobba, and I. N. Hajj, "Static Timing Analysis Including Power Supply Noise Effect on Propagation Delay in VLSI Circuits," in *Proc. DAC*, pp .295–300, 2001.

[8] D. Kouroussis, R. Ahmadi, and F. N. Najm, "Worst-Case Circuit Delay Taking into Account Power Supply Variations," in *Proc. DAC*, pp .652–657, 2004.

[9] S. Pant and D. Blaauw, "Static Timing Analysis Considering Power Supply Variations," in *Proc. ICCAD*, pp .365–371, 2005.

[10] S. Pant, D. Blaauw, V. Zolotov, S. Sundareswaran, and R. Panda, "A Stochastic Approach To Power Grid Analysis," in *Proc. DAC*, pp. 171–176, 2004.

[11] Y. Jiang and K. Cheng, "Analysis of Performance Impact Caused by Power Supply Noise in Deep Submicron Devices," in *Proc. DAC*, pp. 760–765, 1999.

[12] H. S. Kim and D. M. H. Walker, "Statistical Static Timing Analysis Considering the Impact of Power Supply Noise in VLSI Circuits," in *Proc. MTV*, pp. 76–82, 2006.

[13] OPENCORES.ORG, http://www.opencores.org/. in *Proc. ASP-DAC*, pp. 353–358, 2001.

[14] R. M. Sakia, "The Box-Cox transformation technique: a review," *The Statistician*, Vol. 41, pp. 169-178, 1992.

[15] The R Project for Statistical Computing, http://www.r-project.org/.

[16] E. Chiprout, "Fast Flip-chip Power Grid Analysis Via Locality and Grid Shells," in *Proc. ICCAD*, pp. 485–488, 2004.

[17] M. Hashimoto, J. Yamaguchi, and H. Onodera, "Timing Analysis Considering Spatial Power/Ground Level Variation," in *Proc. ICCAD*, pp. 814–820, 2004.

[18] I. T. Jolliffe, "Principal Component Analysis," 2nd Edition, Springer, 2004.

[19] H. Masuda, S. Ohkawa, A. Kurokawa, and M. Aoki, "Challenge: Variability Characterization and Modeling for 65- to 90-nm Processes," in *Proc. CICC*, pp. 593–599, 2005.

[20] P. Ghanta, S. Vrudhula, S. Bhardwaj, and R. Panda, "Stochastic Variational Analysis of Large Power Grids Considering Intra-die Correlations," in *Proc. DAC*, pp. 211–216, 2006.