Measurement and Analysis of Inductive Coupling Noise in 90 nm Global Interconnects

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***Abstract*—Inductive coupling is becoming a design concern for global interconnects in nanometer technologies. We present measurement results of the effect of inductive coupling on timing, and demonstrate that inductive coupling noise is a practical design issue in 90 nm technology. The measured delay change curve is consistent with circuit simulation results for an *RLC* interconnect model, and clearly different from those for a conventional *RC* model. The long-range coupling effect of inductive coupling, and noise reduction caused by ground insertion or decreased driver size were clearly observed on silicon. Examination of noise cancellation and superposition effects shown in measurement results confirm that the summation of delay variations due to each individual aggressor is a reasonable approximation of the total delay variation.**

***Index Terms*—Signal integrity, measurement, inductive coupling noise, interconnect modeling.**

I. Introduction

INTERCONNECT noise is becoming an important issue, and capacitive crosstalk noise is a well-known factor in interconnect delay variation. The nanometer technology regime has raised inductive coupling as a design consideration, and many studies using circuit simulation have been reported [1], [2]. However, simulation models have not been adequately verified, i.e., correlation between simulation and measurement has been reported only in a few papers [3]–[6]. Though [3] demonstrated waveform and interconnect delay with TDR/TDT (time domain reflectometry/transmission) and frequency domain measurement, this has limited application because interconnect structures are very different from practical global interconnects. On-chip waveform measurement circuits have been widely studied recently [4], [7]–[9] with particular focus on power supply noise [7], [8]. However, these circuits are difficult to use for inductive coupling noise because it is much sharper and includes higher frequency components than power supply noise. Ref. [4] implemented on-chip oscilloscope circuits to observe noise waveforms, and observed no inductive coupling effect. Ref. [5] observed inductive and capacitive coupling noise waveforms with sample and hold circuit. However, interconnect modeling for simulation and noise impact on timing were not discussed. Ref. [6] is a work preliminary to this paper. Ref. [9] observed a waveform that overshot due to self inductance, but did not measure coupling noise. Measurement circuits require dedicated analog circuit design and a large chip area. None of the previous papers clearly measured the effect of inductive coupling noise on timing in practical operating conditions, though capacitive coupling noise was reported (e.g., [10]).

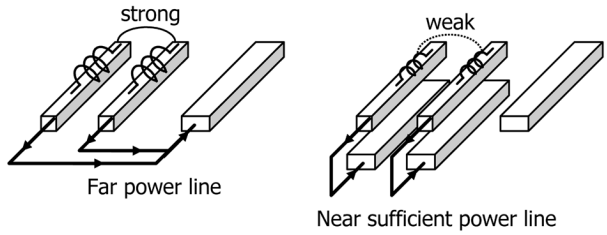

Fig. 1. Dependence of inductive coupling on power lines.

The contributions of this work in 90 nm technology are: 1) measurement of a significant amount of delay variation due to inductive coupling noise in a practical bus structure; 2) verification of an interconnect model for circuit simulation; 3) observation of the long-range effect of inductive coupling; 4) assessment of noise suppression techniques such as increasing ground wires and narrowing the width of signal wires on silicon; and 5) confirmation of the superposition effect of inductive coupling noise. In our primary work [11], we were not able to observe inductive coupling clearly because capacitive coupling noise dominated the inductive coupling noise and the performance and functionality of the measurement circuit was not adequate. For this study, phase interpolators and a bypass circuit were added to the measurement circuitry to make more detailed measurement possible, and wire structures were carefully chosen so that inductive coupling would dominate capacitive coupling.

The remainder of this paper is organized as follows. Section II explains features of the inductive coupling effect. Section III describes measurement circuitry and the interconnect structure. Section IV presents measurement results and a discussion. Section V concludes the paper.

II. Characteristics of Inductive Coupling Noise

This section briefly describes characteristics unique to inductive coupling: dependency on design parameters, long-range ef-

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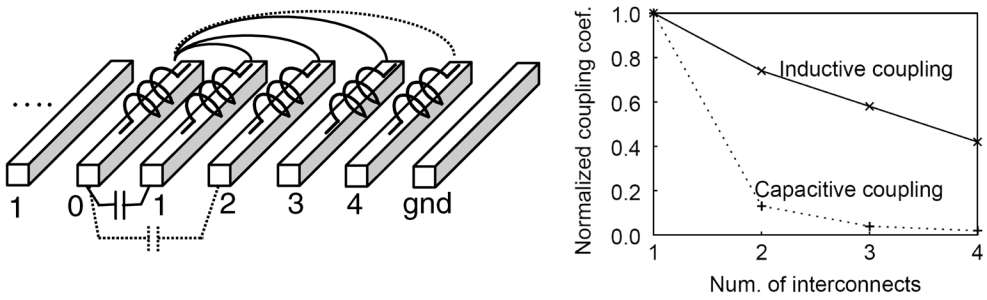

Fig. 2. Long-range effect of inductive coupling.

fect and waveform shape. The superposition effect of inductive coupling noise is also discussed.

The inductive coupling effect is intensified/alleviated by power lines, driver sizing, and interconnect width. Fig. 1 shows the dependence of inductive coupling on power lines. Inductive coupling between two signal lines strongly relies on the overlap of current loops. When power lines are wide and close enough, the current loops become small and the inductive coupling to other signal lines becomes weak.

With small drivers, the inductive coupling effect is smaller, because small drivers inject less current. In [3], the ratio of driver output impedance to characteristic impedance of the interconnect is one of the metrics that indicate whether inductive coupling should be considered or not. Narrower interconnects have larger characteristic impedance, and so they reduce current injected by the driver, which results in smaller inductive coupling noise. In addition, a narrow interconnect with high resistivity attenuates coupling noise.

Fig. 2 depicts the long-range effect of inductive coupling. Capacitive coupling, which is caused by an electric field, is remarkably reduced by distance and signal shield line insertion. Inductive coupling originating from a magnetic field, by contrast, is slowly alleviated by distance and signal line insertion. The graph on the right side of Fig. 2 is an example of the coupling coefficient between interconnect 0 and interconnects 1 through 4 in the bus structure shown in Fig. 2. Interconnect length, width, thickness, and spacing are set to 1400 μm, 4 μm, 0.9 μm, and 4 μm, respectively, and the width of the ground wire is 10 μm. The interconnect 1 through 4 and the ground interconnects are placed symmetrically on both sides of wire 0. Vertical interconnects are placed in the upper and lower layers in 100% track utilization. We can clearly observe both capacitive and inductive coupling noise waveform with this structure in simulation. The coupling coefficients are normalized by the coefficient of interconnect 1. The decrease in the inductive coupling coefficient with distance is slower than that of the capacitive coupling coefficient, and the long-range effect of inductive coupling is remarkable. The inductive coupling effect can thus be increased by superposition of noise waveforms from many aggressors.

Fig. 3 shows an example of a noise waveform considering capacitive and inductive coupling. The interconnect structure is the same as in Fig. 2. The size of the interconnect drivers is set to 32X, which corresponds to 120 Ω output resistance. A sharp spike mainly caused by inductive coupling first appears in Fig. 3, followed by a gentle bump caused by capacitive coupling.

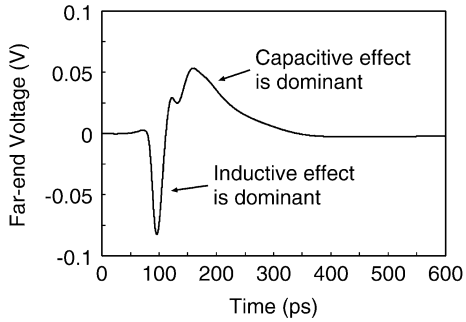

Fig. 3. A coupling noise waveform.

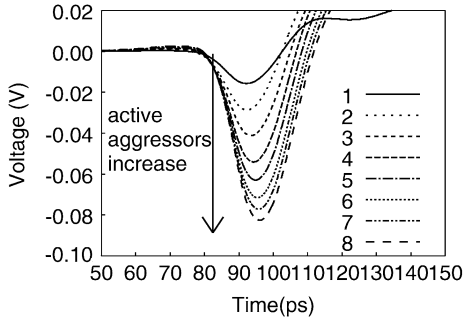

Fig. 4. Overlapped noise waveform simulated with resistive drivers. Number of key is number of active aggressors. Each aggressor makes rise transition at same timing.

The inductive effect is observed in a much shorter time than the capacitive effect, so inductive coupling causes delay variations in the short term range. The sharpness of the spike makes it difficult to measure inductive coupling noise.

Because of the long-range effect, the inductive coupling effect from many aggressors overlaps and is escalated. Fig. 4 shows an example of overlapped noise waveforms. The interconnect structure in Fig. 2 is used for simulation. Interconnects are driven by 32X (120 Ω) inverters and terminate in 4X inverters. The peak noise voltage increases as the number of active aggressors increases. In a linear circuit, the peak noise voltage of an overlapped noise waveform can be computed by summing up each individual noise peak. This superposition holds reasonably well even in a nonlinear circuit as long as the noise magnitude is not very large [12], [13].

As with the peak noise voltage, we expected that the total delay variation due to noise could be estimated by summing up

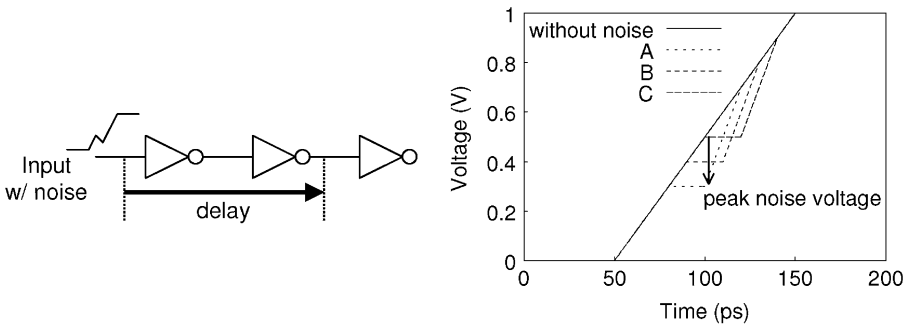

Fig. 5. Simulation setup of Fig. 6. Figure on left is circuit for simulation. All inverters are same size. Graph on right is inverter input voltage waveform of the three graphs in Fig. 6.

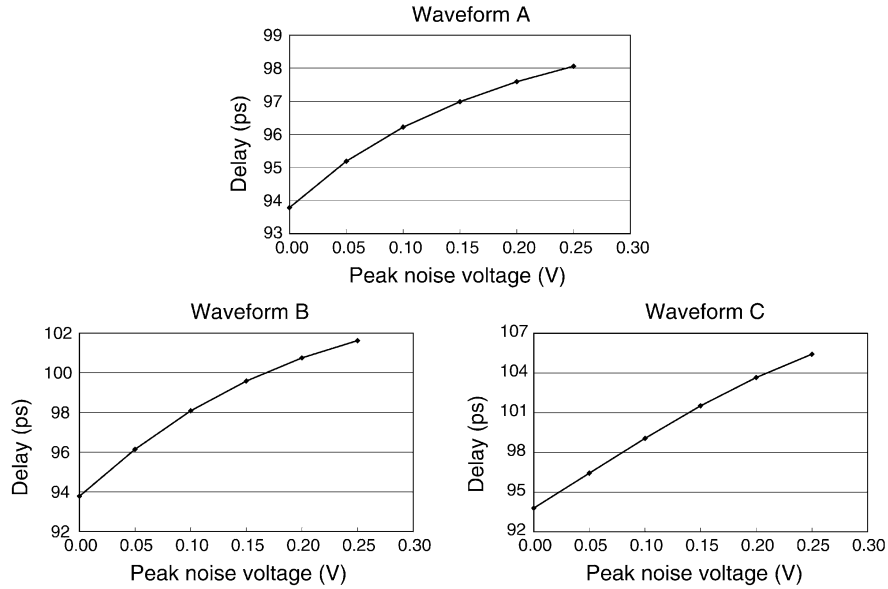

Fig. 6. Noise peak voltage of inverter input and propagation delay in simulation. X axis is the peak noise voltage.

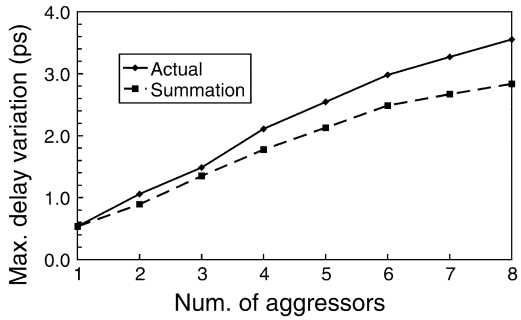

Fig. 7. Interconnect delay variation due to inductive coupling noise was simulated with MOS drivers. Delay variation of overlapped noise, and summation of delay variation due to each individual noise are compared.

the delay variation caused by each aggressor. We confirmed this estimate experimentally by simulating the circuit on the left of Fig. 5. The rise signal waveform with noise is input to the first inverter, and the propagation delay from 10% of the first inverter input to 90% of the second inverter output is observed. The input waveform is depicted on the right side of Fig. 5. We used three rise input waveforms with different noise injection timings. Fig. 6 shows relations between the peak noise voltage and the propagation delay for each input waveform. These results indicate that the propagation delay increases approximately in proportion to the peak noise voltage. Intuitively, we attribute this to the fact that, in nanoscale devices, the nMOS saturation current is mostly proportional to V_{gs}, i.e., the gate input voltage. Gate delay is the time required to discharge, and the noise reduces its discharging current. Thus, the noise area, in other words the integral of noise voltage with respect to time, corresponds to increase in delay. In the current setup, the noise area is proportional to the noise peak voltage, and thus the increase in delay is roughly proportional to the noise peak voltage.

Fig. 7 shows the actual delay variation due to multiple aggressors and the summation of delay variation caused by each aggressor. The simulation setup is the same as that in Fig. 4. The delay variation depends on aggressor and victim transition timing. We evaluated the maximum delay variation. The summation of the delay variation by each aggressor is well correlated with the actual maximum delay variation. A difference above five aggressors is thought to mainly come from nonlinearity of MOS transistors.

The noise superposition can cause the cancellation of noise as well as intensification of noise. When an aggressor makes a rise transition and another aggressor makes a fall transition, the noises from the two aggressors may cancel each other. Fig. 8 shows simulation results of the noise cancellation effect. Four aggressors make rise transitions and the other zero to four aggressors make fall transitions. The simulation setup is the same

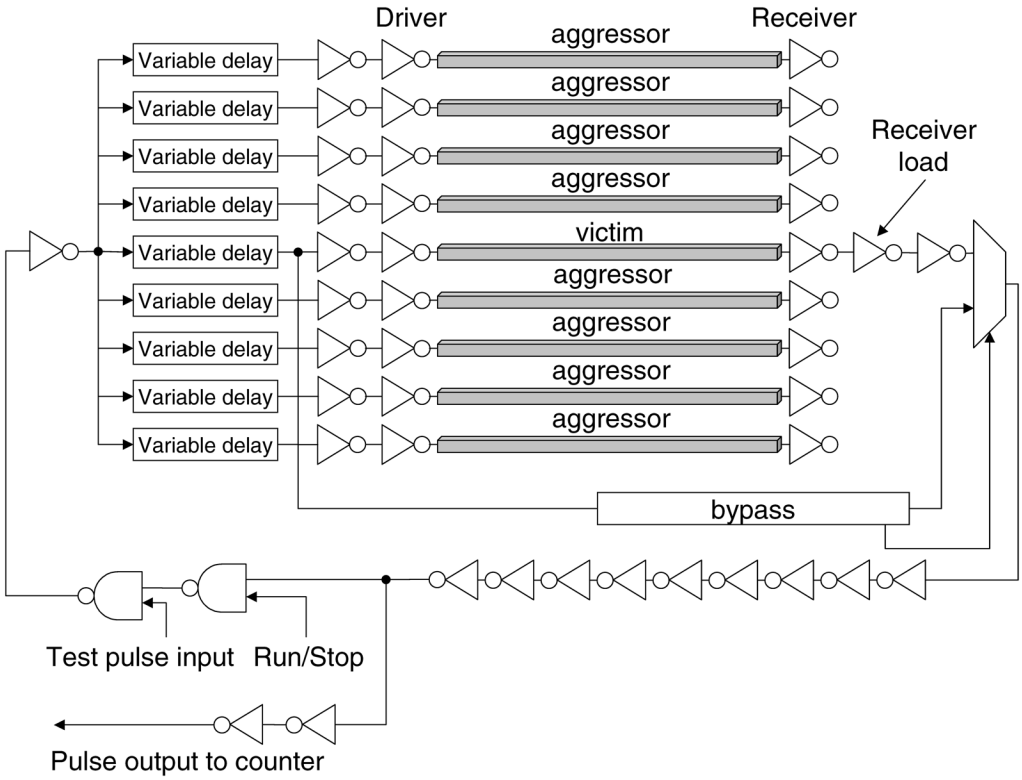

Fig. 9. Measurement circuit structure.

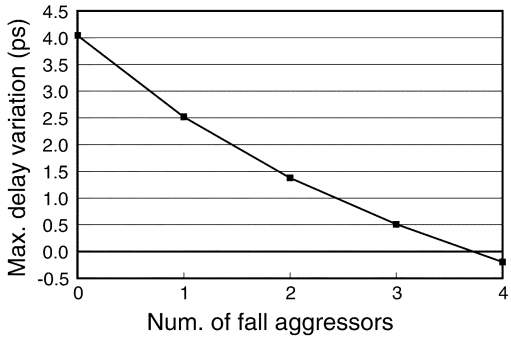

Fig. 8. Simulated noise cancellation effect.

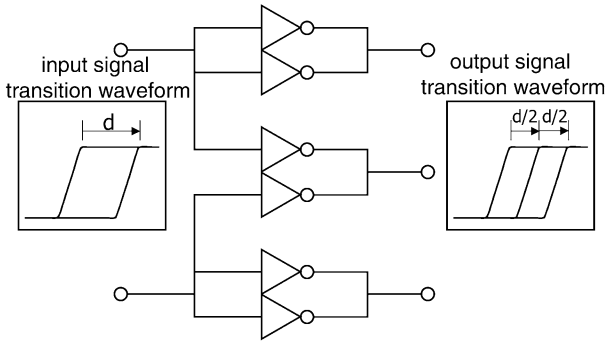

Fig. 11. Phase interpolator.

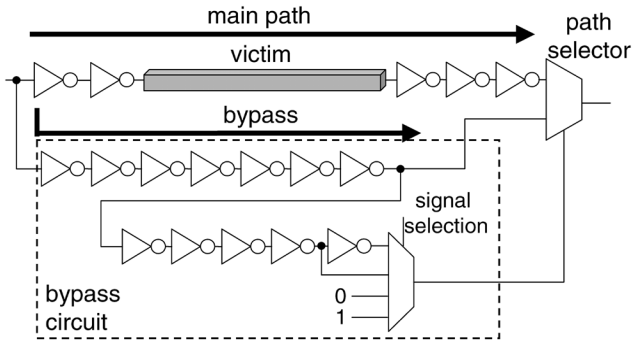

Fig. 10. Bypass circuit.

as that in Fig. 7. The increase in delay caused by the four rise aggressors is cancelled by the fall aggressors, and noise cancellation occurs.

III. Measurement Circuit Structure

A. Measurement Circuitry

Fig. 9 shows the circuit designed to measure interconnect delay variation due to inductive coupling noise. The measurement circuit consists of a victim and eight aggressors in a bus-structure, a ring oscillator, a bypass circuit, a counter, and variable delay circuits.

Delay variation of the victim due to coupling noise is measured by the counter as cycle time variation of the ring oscillator. The victim is embedded in the ring oscillator, and rise and fall signals are input to the victim alternately. The observed ring oscillator cycle includes the average of rise and fall signal delays. By using the bypass circuit (Fig. 10), delay variations for rise and fall transitions at the victim are measured separately. The bypass circuit generates a bypass delay that is not affected by

Interconnect length	1310 μm
Interconnect width	1 μm
Interconnect pitch	5 μm
Driver size	32X (≒120Ω)
Receiver	4X
Receiver load	1X

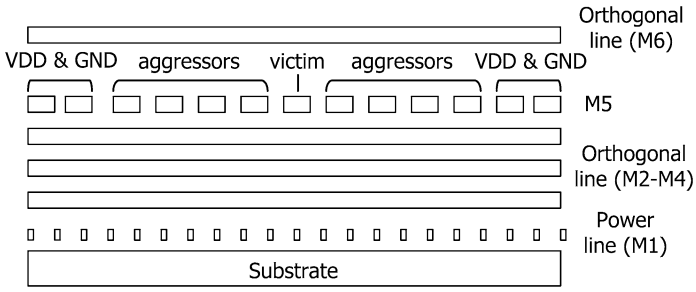

Fig. 12. Interconnect cross section.

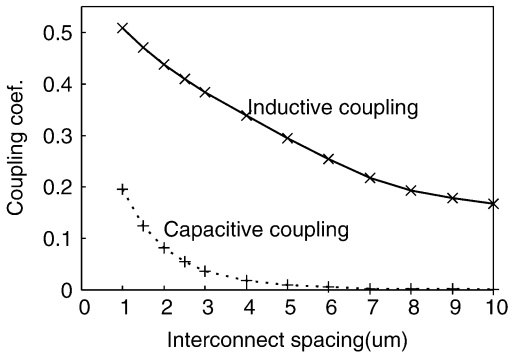

Fig. 13. Interconnect spacing and coupling coefficient. Inductive and capacitive coupling coefficients are normalized with coefficients at 1 μm spacing respectively.

crosstalk noise. The path selector chooses the main path delay or the bypass delay according to the type (rise/fall) of transition, and then only the rise or fall delay is captured into the counter while the other is discarded.

Relative transition timing between the victim and aggressors is changed with the variable delay circuits. A variable delay circuit consists of a phase interpolator (Fig. 11) [14] and cascaded inverters with a selector. The cascaded inverters insert the delay of up to 15 inverters (about 200 ps), which is a sufficiently wide timing range for the measurement. The delay variation appears in a short timing range because of the sharp spike waveform of inductive coupling noise, and so transition timing must be controlled by a small time step. To generate finer aggressor timing than a two-stage inverter delay $(2t_{\rm inv})$, we introduced a two-stage phase interpolator that divides $2t_{\rm inv}$ by four. The aggressor timing can thus be controlled by $t_{\rm inv}/2$.

In our implementation, the control and counter signals are stored in scan-chained flip-flops. This makes it easy for a pattern generator and a logic analyzer to measure them because all signals are digital and the IO speed of a few MHz is fast enough.

B. Interconnect Structure and TEG Variations

Fig. 12 shows the interconnect cross section of the bus structure, and summarizes basic parameters. We based the length and width of our interconnects on those of actual global interconnects with repeater insertion in current use. To clearly observe delay variation due to inductive coupling noise, we determined the parameters such that inductive coupling dominates capacitive coupling. A large enough driver which can increase inductive coupling noise was adopted. To reduce side-wall coupling capacitance, non-thick metal layer (M5) are selected for bus lines. A interconnect spacing is set to 4 μm which is wide enough to reduce capacitive coupling. Fig. 13 shows the relation between coupling coefficients and interconnect spacing. Wide spacing decreases both capacitive and inductive coupling coefficients. However, capacitive coupling is more sensitive to spacing than inductive coupling, and wide spacing relatively increases inductive coupling effect.

The following summarizes the variations in TEGs.

TEG_STD
: The basic structure TEG with parameters shown in Fig. 12.

TEG_M2POWERLINE
: Parallel power lines with $\mathrm{width} = 2\,\mu$m and $\mathrm{pitch} = 5\,\mu$m are located in the M2 layer.

TEG_NARROWWIRE
: Interconnect width is narrowed to 0.14 μm.

TEG_SMALLDRIVE
: Driver size is decreased to 8X.

TEG_LARGELOAD
: Receiver load is increased to 32X.

TEG_NODECAP
: Decoupling capacitances near the drivers are removed.

TEG_STD is designed to measure clearly the delay variation due to inductive coupling. TEG_M2POWERLINE, TEG_NARROWWIRE, and TEG_SMALLDRIVE are intended to measure the alleviation of the inductive coupling effect. TEG_LARGELOAD is intended to evaluate how the receiver loading affects the delay change curve. TEG_NODECAP is intended to determine whether existence of decoupling capacitance very close to the drivers affects inductive coupling noise.

The chip shown in Fig. 14, with supply voltage of 1.0 V, was fabricated in a 90 nm CMOS process with six metal layers.

IV. Measurement Results

A. Measurement and Simulation Setup

Delay variation is computed based on the measured ring oscillator cycle. An average of five measurements is adopted for cycle time. The delay variation shown in this paper represents the averaged results for three chips. The standard deviation of 200 measurement results is 0.355 ps, which demonstrates that our measurements have good reproducibility enabling accuracy of several ps of delay variation. The cycle time variation was also measured varying the delay of variable delay circuit in victim without aggressor operation. We then know the relative transition timing of aggressors and victim on the assumption

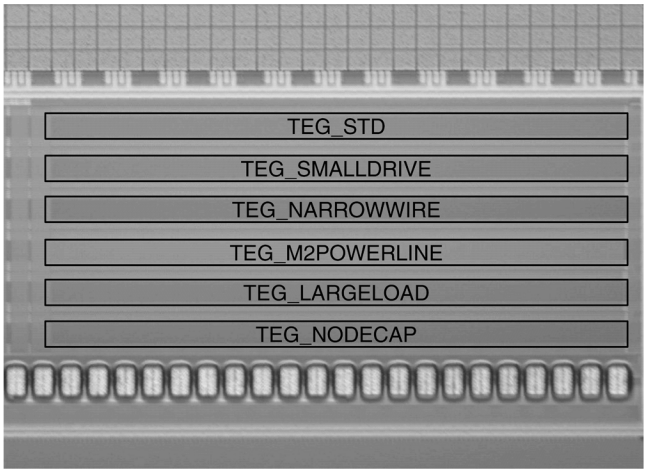

Fig. 14. Microphotograph of fabricated chip.

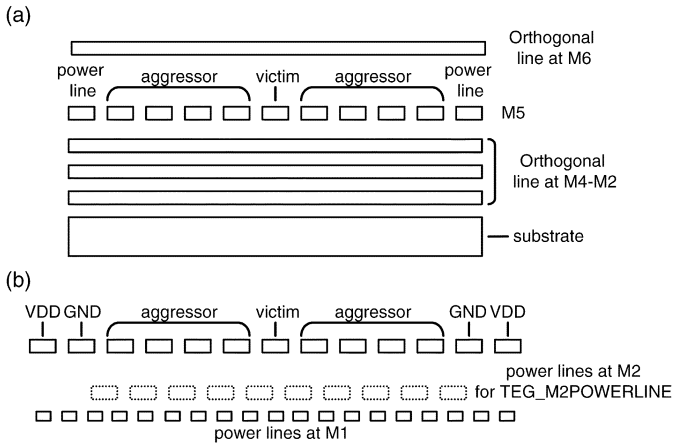

Fig. 15. Interconnect structure for *RLC* extraction.

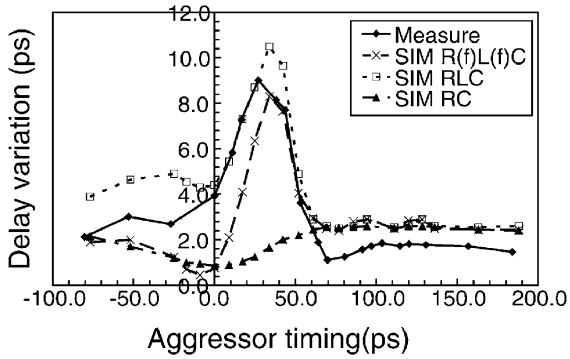

Fig. 16. Delay change due to coupling noise on TEG_STD.

that the delays of variable delay circuits in aggressors are identical to that in victims.

We compared measurement results with circuit simulation results using three interconnect models: 1) the *RLC*-distributed constant model with frequency dependency (*R(f)L(f)C* model); 2) the *RLC*-distributed constant model without frequency dependency (*RLC* model); and 3) the *RC*-distributed ladder model (*RC* model).

Resistance *R*, capacitance *C*, and inductance *L* of interconnects were extracted by a 3-D field solver. We selected Raphael [15] as the 3-D field solver. *R* and *L* are extracted with Raphael RI3 program, and *C* is extracted with Raphael RC3 program. The interconnect structures for *RL* and *C* extraction are shown in Fig. 15(a) and (b), respectively. Power lines parallel to aggressors and victim at M5 and M1 layers are considered as a current return paths, and M2 lines are also considered in TEG_M2POWERLINE. In capacitance extraction of TEG_M2POWERLINE, M2 lines are placed parallel to M5 lines. To reduce the extraction time, unnecessary interconnects are removed in *RL* and *C* extraction structures. Lines orthogonal to victim and aggressors are ignored in *RL* extraction because they does not affect the extracted inductance. Substrate is not also considered in *RL* extraction, because wires in the first layer run in parallel to bus wires, and magnetic field is shielded. M1 lines are omitted in capacitance extraction because they are near to substrate and the impact on the extraction results is small.

For the *R(f)L(f)C* and *RLC* models, we adopt the W-element interconnect model [16], [17] which can model the frequency dependency of the interconnect. Resistance and inductance are frequency-dependent parameters [18], and frequency dependency of *R* and *L* is modeled with W-element in the *R(f)L(f)C* model. As for frequency independent parameters, such as *R*, *L*, and *C* in *RLC* model and *C* in *R(f)L(f)C* model, interconnects are assumed to have the constant values in all frequency range. *R* and *L* values are frequency dependent fundamentally, and *R* and *L* values at 17 GHz (significant frequency component of the driver inputs [19]) were used in the circuit simulations with *RLC* model.

We also took the power supply network on chip into account, and simulated delay variation of ring oscillator and interconnect due to power supply noise. The measured package and bonding wire inductance were attached, and the on-chip power/ground wires were carefully modeled as resistance based on the layout pattern.

B. Verification of Inductive Coupling Effect

Fig. 16 shows delay variation when all aggressors and victim make a rise transition. The delay variation is the amount of delay increase or decrease from the delay excluding aggressor operation. Relative transition timing between victim and aggressors is changed where all aggressors change simultaneously. In this case, delay variation due to inductive coupling is expected to be observed as a delay increase. Capacitive coupling cause delay decrease in this switching pattern, and we can easily separate the inductive coupling effect from capacitive coupling effect. There is a remarkable difference between *RC* and *RLC/R(f)L(f)C* models in the range from 20 to 60 ps aggressor timing, which arises from the consideration of inductive coupling. The curve of the measurement result follows the simulation result with both the *RLC* and *R(f)L(f)C* model. This result reveals that inductive coupling considerably affects interconnect delay in 90 nm technology. Inductive coupling effect in high performance interconnects increases in more advanced processes [20], and it will be a serious problem in the future. This result also indicates that the *RLC* and *R(f)L(f)C* distributed constant model are effective for noise-aware timing analysis. From now, we demonstrate simulation results of the *RLC* model only since there is not a significant

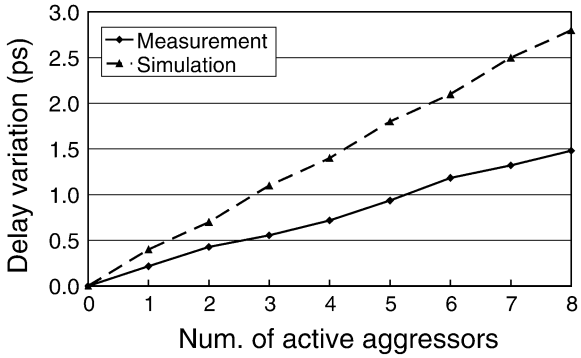

Fig. 17. Measurement results for delay change on TEG_STD at aggressor timing = 180 ps.

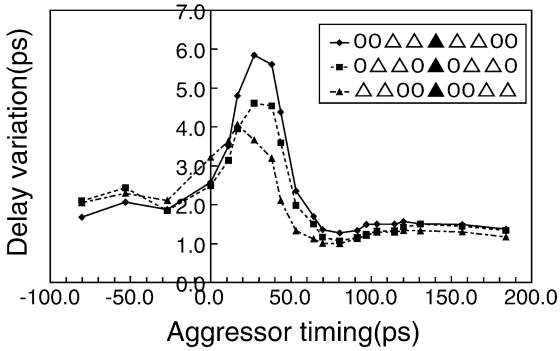

Fig. 19. Measurement result for delay change when four near/far aggressors are active. "0" is an inactive aggressor, and "△" is an active aggressor. "▲" at the center corresponds to the victim.

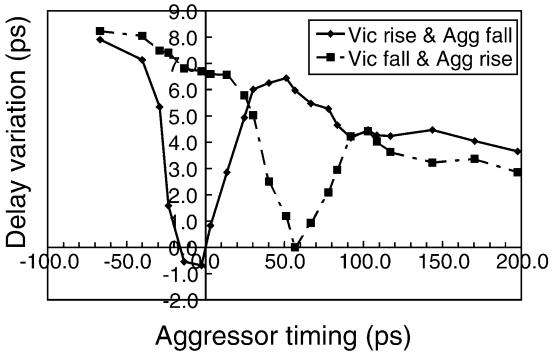

Fig. 18. Measurement results for delay change on TEG_STD. Transition directions of aggressors are opposite to those of the victim.

difference between the *RLC* and *R(f)L(f)C* models. Delay variations in the ranges of below 0 ps and over 60 ps aggressor timing are found in both measurement and *RLC* simulation results. The effect of crosstalk noise does not affect this range, and this delay variation is due to power supply noise by aggressors. Fig. 17 indicates that increase in delay at aggressor timing = 180 ps, where the aggressor and victim transitions are not overlapped, is proportional to the number of active aggressors and indicates that delay is slightly increased by power supply noise. The absolute error between simulation and measurement results is sufficiently small. We see 1.5 ps delay increase in measurement and 2.8 ps delay increase in simulation at aggressor timing = 180 ps. More accurate simulation is difficult since accurate power grid and model with implicit parasitic elements in addition to MOS and wire models is necessary, but it is hardly obtained with available information given from the foundry.

We next changed the transition direction between the aggressors and the victim, and measured the delay change curve. Fig. 18 includes two curves; victim rise and aggressor fall, and victim fall and aggressor rise. As the transition timings approach each other, the delay variation decreases, which is different from Fig. 16. This decrease in delay demonstrates that delay variation is caused by inductive coupling, because capacitive coupling and power supply noise should increase delay in this setup. The bypass circuit in Fig. 10 enabled us to measure two delay change curves for rise and fall transitions separately. The rise and fall input delays of the variable delay circuit are different. The difference between rise and fall delays causes mismatching of relative timing between aggressors and victim in the ring oscillator measurement where rise and fall signals are input alternately. To solve this problem, separate measurement of rise and fall delays is needed.

C. Evaluation of Inductive Coupling Characteristics

Fig. 19 demonstrates the long-range effect of inductive coupling. We measured the delay variation caused by four active aggressors varying active aggressor positions. As the active aggressors become distant, the delay variation decreases, but it decreases slowly. Even when there are two quiet wires between the active aggressors and the victim, the delay variation is only reduced by half, because inductive coupling is not easily shielded by signal lines and is slowly weakened by distance.

Figs. 20–24 demonstrate the degree to which noise suppression techniques and design parameters influence delay variation comparing with TEG_STD.

(a) Adding parallel ground wires in the lower layer (TEG_M2POWERLINE) reduces delay variation by 3 ps, because inductive coupling becomes weaker.
(b) Narrowing signal interconnects (TEG_NARROWWIRE) decreases delay variation by 4 ps, because higher resistance of narrower wires damps inductive effects.
(c) Reducing driver sizes (TEG_SMALLDRIVE) decreases delay variation, because a driver with high output impedance injects less voltage and current into interconnects.
(d) Enlarging receiver loading (TEG_LARGELOAD) increases susceptive timing range, because a slower receiver transition widens the range of timing that can be affected by inductive noise.
(e) Reducing adjacent decoupling capacitance (TEG_-NODECAP) scarcely affects measurement results.

The above measurements (a)-(d) agree with the qualitative discussion and circuit simulation, which shows that noise suppression techniques developed based on simulation will be effective. For a practical use of these techniques, tradeoff between reduction of delay variation and increase of delay or routing cost should be carefully examined.

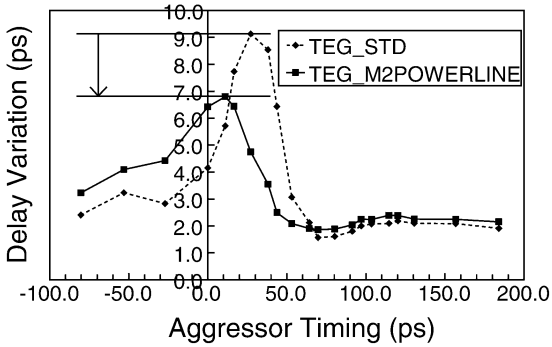

Fig. 20. Measurement of TEG_M2POWERLINE. Parallel wires in M2 weaken inductive coupling.

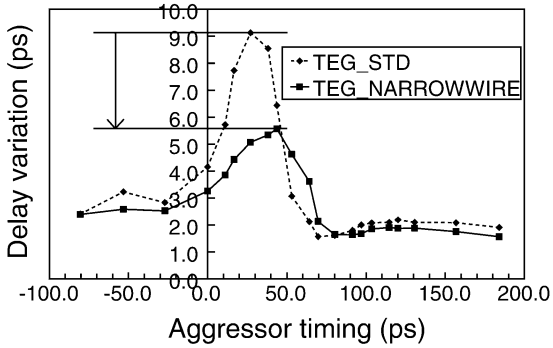

Fig. 21. Measurement of TEG_NARROWWIRE. Narrow signal wires damp inductive noise.

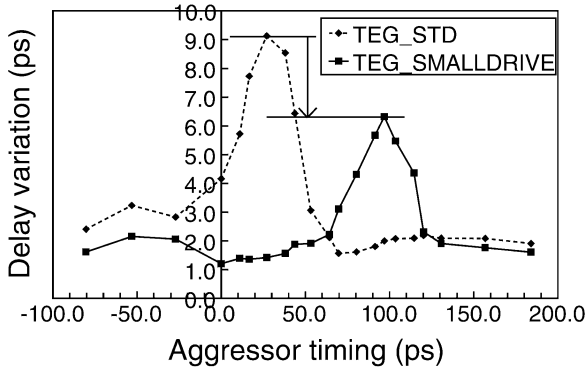

Fig. 22. Measurement of TEG_SMALLDRIVE. Small driver injects less noise.

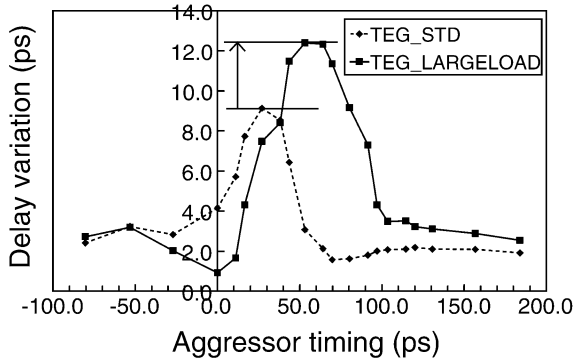

Fig. 23. Measurement of TEG_LARGELOAD. Large receiver load enlarges noise susceptive timing.

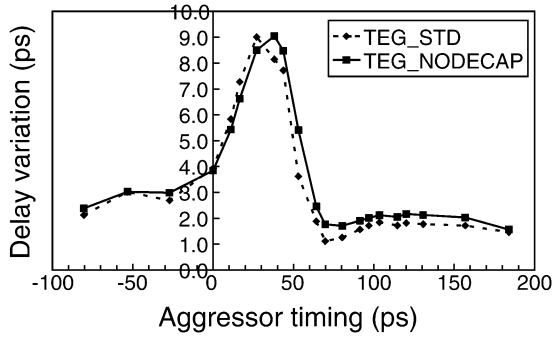

Fig. 24. Measurement of TEG_NODECAP.

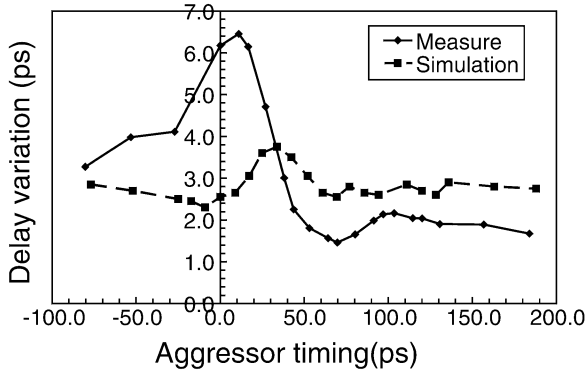

Fig. 25. Comparison between measurement and simulation results of TEG_M2POWERLINE.

We also compare measurement results and the simulation results of TEG_M2POWERLINE, TEG_NARROWWIRE, TEG_SMALLDRIVE, and TEG_LARGELOAD (Figs. 25–28). We adopt *RLC* model for interconnect modeling in simulation because the difference between *RLC* and *R(f)L(f)C* model were small. In TEG_NARROWWIRE, TEG_SMALLDRIVE, TEG_LARGELOAD, simulation results are consistent with the measurement results, and validity of simulation model are proven. The effect of inductive coupling noise in TEG_M2POWERLINE in simulation is smaller than measurement results. A possibility is that the resistivity of manufactured M2 lines was higher than we expected. In this case, less return current would flow in the M2 lines, and inductive coupling was not weakened as much as we expected.

We have extracted *RLC* parameters of TEGs for simulation, and here we review the *RLC* parameters of the TEGs. The extracted interconnect parameters are shown in Table I. The characteristic impedance is calculated as $\sqrt{|(R+j\omega L)/(j\omega C)|}$, where $\omega = 2\pi\times$ 17 GHz. Inductive coupling coefficient between a victim and a adjacent aggressor in TEG_STD was 0.338, and was reduced to 0.123 in TEG_M2POWERLINE where inductive coupling effect was reduced. Characteristic impedance Z_0 and resistance $R_{\rm wire}$ of interconnects on TEG_STD was 239 and 157 Ω. $R_{\rm wire}$ are 994 Ω and Z_0 increased to 755 Ω in TEG_NARROWWIRE where high $R_{\rm wire}/Z_0$ ratio reduces the inductive effect [3]. Increase of L (1.08 to 1.36 nH) and decrease of C (163 to 103 fF) also slightly contributes the increase of Z_0 in this TEG.

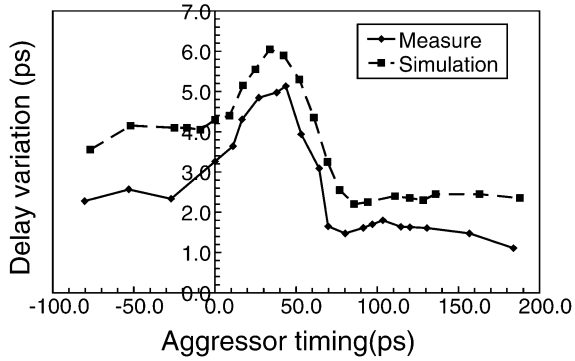

Fig. 26. Comparison between measurement and simulation results of TEG_NARROWWIRE.

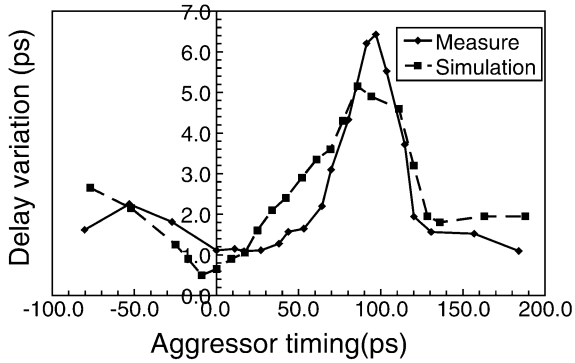

Fig. 27. Comparison between measurement and simulation results of TEG_SMALLDRIVE.

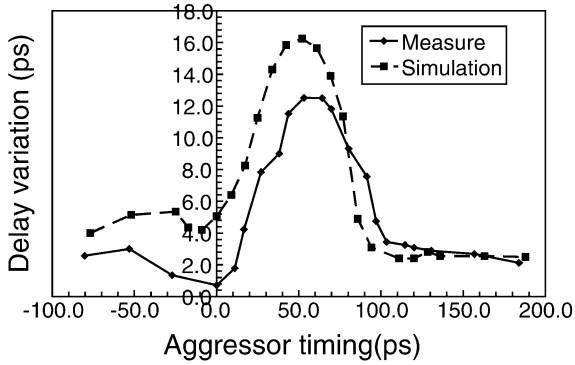

Fig. 28. Comparison between measurement and simulation results of TEG_LARGELOAD.

In TEG_SMALLDRIVE where small driver restricts current injected to interconnects, driver resistance $R_{\rm driver}$ was increased from 120 Ω to 500 Ω, and $Z_0/R_{\rm driver}$ was reduced to 2.00 from 0.48. The variation of these interconnect parameters causes the change in inductive coupling noise discussed so far.

D. Noise Superposition

Here, we discuss the superposition of the inductive coupling effect. Delay variation can be intensified/weakened by multiple aggressors based on their transition directions. We first show the cancellation effect by aggressors whose transition directions are opposite. We next present measurement results that show

TABLE I
EXTRACTED INTERCONNECT PARAMETERS. R, L, C, Z_0 ARE RESISTANCE, SELF-INDUCTANCE, CAPACITANCE, AND CHARACTERISTIC IMPEDANCE OF THE VICTIM. K_L IS INDUCTIVE COUPLING COEFFICIENT BETWEEN A VICTIM AND AN ADJACENT AGGRESSOR

TEG	R (Ω)	L (nH)	C (fF)	$Z_0(\Omega)$	K_L
TEG_STD	157	1.08	163	239	0.338
TEG_M2-POWERLINE	150	0.78	162	233	0.123
TEG_NARR-OWWIRE	994	1.36	103	755	0.267

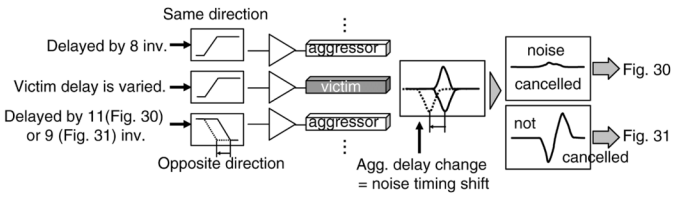

Fig. 29. Measurement setup of Figs. 30 and 31. Same and opposite direction transition are input to aggressors to observe noise cancellation effect.

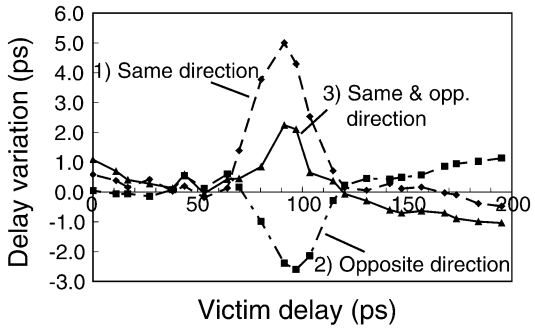

Fig. 30. Measurement results when aggressors make same and/or opposite direction transition.

that the total timing variation by multiple aggressors can be estimated by the summation of timing variation due to each aggressor.

1) Cancellation Effect: We observed the cancellation effect using the measurement setup in Fig. 29. Four aggressors on one side make the same direction transition as the victim, and four aggressors on another side make the opposite transition. The timing of aggressors is fixed, and that of victim is varied. We measured the fall delay variation for victim using the bypass circuit.

Fig. 30 shows three delay variation curves measured with the TEG_STD on the test chip:

1) aggressors with the same direction operate;
2) aggressors with the opposite direction operate;
3) both same and opposite direction aggressors operate.

The X axis represents the delay of the victim input signal. We can see the delay increase in curve 1) and decrease in curve 2) caused by inductive coupling noise. On the other hand, a smaller delay increase is observed in curve 3), which indicates partial cancellation of inductive coupling noise when the aggressors transition in opposite directions. We clearly observed a decrease in inductive coupling noise caused by aggressors transitioning in opposite directions on silicon.

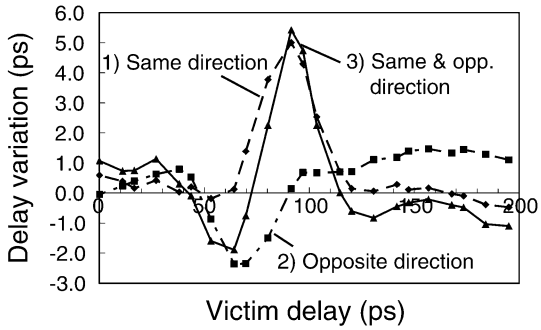

Fig. 31. Timing of opposite direction transition is shifted from Fig. 30.

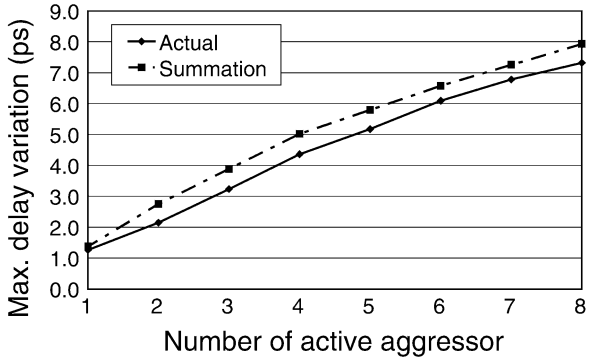

Fig. 32. Measured maximum delay variation due to inductive coupling. Delay variations of overlapped noise and summation of individual noises are compared.

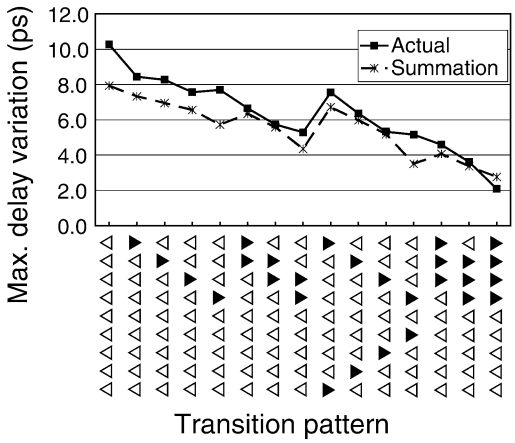

Fig. 33. Measured maximum delay variation due to inductive coupling including opposite direction transitions. Delay variations of overlapped noise and summation of each individual noise are compared.

Fig. 31 shows three delay variation curves that are very similar to those in Fig. 30. The difference is that the transition timing of opposite transition aggressors is advanced by a two-stage inverter delay. Curves 1) and 2) show delay increase and decrease similar to those in Fig. 30. As for curve 3), both a delay increase and decrease caused by the same and opposite transition are observed. This is because inductive coupling noises from the two sources do not overlap each other because of the timing shift depicted in Fig. 29. The timing shift of the two-stage inverter delay corresponds to 25 ps, and the noise cancellation occurs only in a narrow timing range.

2) Superposition of Noise Effect: To reduce the capacitive coupling effect, prohibition of particular switching patterns is discussed, and several bus encoding techniques have been proposed [21]–[23]. However, applying these techniques to inductive coupling is very difficult, because the coupling effect from many far aggressors must be considered. In the case of capacitive coupling, only adjacent aggressors are considered, and the number of switching patterns is limited. In contrast, the number of switching patterns for inductive coupling can exponentially increases with respect to the number of aggressors. For example, there are 4^9 switching patterns in a nine-line structure. Though the switching pattern might be reduced due to symmetry, verifying every pattern using circuit simulation is still impractical.

Here, we demonstrate that the inductive coupling noise effect by multiple aggressors on timing can be reasonably approximated with summation of delay variation due to each aggressor based on measurement results. This approximation enables us to determine which switching patterns may cause unacceptable delay variation. As discussed in Section II, the overlapped crosstalk noise effect is equal to the summation of each individual crosstalk noise in a linear circuit, but the nonlinearity of MOS characteristics may disrupt this law. However, linear approximation can be effective as long as noise amplitude is small.

Fig. 32 is a measurement result for delay variation due to inductive coupling. Actual delay variation due to multiple aggressors and summation of delay variation due to each aggressor are compared. We can see that the two curves are well correlated. This result indicates that delay variation due to multiple aggressors can be estimated by summing delay variation by each aggressor with a reasonable accuracy. Fig. 33 shows the delay variation with various input patterns. The X axis represents the transition pattern. △ and ▼ are rise and fall transitions, respectively. In each column, the center symbol is the victim, and the other eight symbols correspond to eight aggressors. There are a huge number of switching patterns, and we selected 15 dissimilar and asymmetrical transition patterns and measured the rise delay variation at the center. The curve of summation closely follows the curve of the actual variation in Fig. 33. The measurement results show that the summation of each individual noise effect can approximate the actual overall noise effect, including the cancellation effect.

V. Conclusion

In summary, we measured a significant effect of inductive coupling on timing in 90 nm global interconnects and demonstrated that inductive coupling has become a practical design issue in advanced technologies. We evaluated interconnect models, *RLC*-distributed constant model gives a good correlation with measurement results. We also verified characteristics unique to inductive coupling, such as the long-range effect and the shielding effect caused by ground wires on silicon. Mitigation techniques for inductive coupling with power lines, driver sizing, and narrowed wire were verified by measurement results. The superposition and cancellation effects were accurately observed on silicon, and measurement results indicated that delay variation by multiple aggressors can be estimated

with acceptable accuracy based on the summation of delay variations from each aggressor.

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