# Quantitative Prediction of On-Chip Capacitive and Inductive Crosstalk Noise and Tradeoff between Wire Cross-Sectional Area and Inductive Crosstalk Effect

Yasuhiro OGASAHARA[†a)], *Student Member*, Masanori HASHIMOTO[†], *and* Takao ONOYE[†], *Members*

**SUMMARY**   Capacitive and inductive crosstalk noises are expected to be more serious in advanced technologies. However, capacitive and inductive crosstalk noises in the future have not been concurrently and sufficiently discussed quantitatively, though capacitive crosstalk noise has been intensively studied solely as a primary factor of interconnect delay variation. This paper quantitatively predicts the impact of capacitive and inductive crosstalk in prospective processes, and reveals that interconnect scaling strategies strongly affect relative dominance between capacitive and inductive coupling. Our prediction also makes the point that the interconnect resistance significantly influences both inductive coupling noise and propagation delay. We then evaluate a tradeoff between wire cross-sectional area and worst-case propagation delay focusing on inductive coupling noise, and show that an appropriate selection of wire cross-section can reduce delay uncertainty at the small sacrifice of propagation delay.

*key words:   signal integrity, interconnect delay, capacitive crosstalk, inductive crosstalk*

## 1. Introduction

In nano-meter technologies, interconnect delay dominates gate delay and accurate estimation of interconnect delay has become an important design issue. Capacitive and inductive crosstalk is a well-known obstacle for accurate interconnect delay estimation. Capacitive crosstalk is widely considered in current designs, whereas inductive crosstalk noise emerges in recent processes. Qualitative discussion generally shows that both capacitive and inductive crosstalk noises will be more significant as the fabrication processes advance, though a paper reports that impact of capacitive crosstalk is reduced in most of shortened interconnects [1]. Technology advancement increases capacitive crosstalk noise owning to a larger aspect ratio of interconnects and sharper signal transition waveforms. In wide and fat global interconnects, fast transitions including higher signal frequency component strengthen inductive crosstalk effect.

Crosstalk noise has been widely discussed based on formulas and simulations [1]–[3], and verified with measurement results [4]–[6]. However, a quantitative prediction considering both capacitive and inductive crosstalk noises in the future has not been reported, as far as the authors know, in spite of its increasing importance.

The contributions of this paper are summarized as follows: 1) predicting capacitive and inductive crosstalk noises in the future processes and 2) revealing that delay uncertainty due to inductive coupling can be mitigated by adjusting wire cross-sectional area with a small delay penalty.

This paper quantitatively predicts the impact of capacitive and inductive crosstalk noise in predictive technologies with circuit simulation. We assume that process parameters, such as transistor performance and power supply voltage, follow ITRS prediction [7], [8].

We also evaluate a tradeoff between wire cross-sectional area and propagation delay focusing on inductive coupling noise, because the prediction suggests that the interconnect resistance significantly influences both inductive coupling noise and propagation delay. There are several past works for crosstalk reduction that discuss adjusting interconnect spacing for capacitive noise [9], differential signaling [3], and noise immunity design in a processor design [10]. We, in this paper, focus on mitigation of inductive crosstalk effect by narrowing interconnect. A careful selection of wire cross-section reduces inductive coupling without much degrading the worst-case propagation delay. By cross-sectional area tuning, the consideration of inductive coupling, which includes inductance extraction involving large matrix computation, becomes unnecessary without modified design procedure and new design tools.

The remaining of this paper is organized as follows. Section 2 qualitatively discusses crosstalk noise on global interconnects. Section 3 describes assumed scenarios of technology advance for crosstalk prediction. Section 4 presents quantitative prediction of capacitive and inductive crosstalk. Section 5 discusses wire cross-section and crosstalk-induced delay. Finally Sect. 6 concludes this paper.

## 2. Qualitative Discussion on Crosstalk Noise

In this section, we explain transmission line effects of interconnects. The characteristics of capacitive and inductive crosstalk noise and their increase due to process scaling are also described.

### 2.1 Transmission Line Effects of Global Interconnects

Transmission line effects should be considered in a long

interconnect when signal rise time is short [11]. The interconnect considered as a transmission line is represented as an RC or RLC distributed circuit in circuit simulation, and its current return path has to be appropriately modeled for RL extraction. An approach to determine driver size is impedance matching between driver output resistance and interconnect characteristic impedance. When the characteristic impedance is equal to the driver resistance and the driver is a CMOS gate, 50% of supply voltage is injected to the interconnect. MOS termination, which is open-end when the receiver is a CMOS gate, doubles the voltage at the end of the interconnect, and a sufficient voltage to sense is input to the receiver. Signal attenuation is also an important characteristic for a long interconnect. The injected signal is attenuated to $e^{-\alpha l}$, where $\alpha$ is attenuation constant and $l$ is interconnect length.

## 2.2 Crosstalk Noise and Process Advancement

Capacitive crosstalk arises from a coupling capacitance between interconnects. In the case of two coupled interconnects as shown in Fig. 1, a signal transition on one interconnect induces a voltage fluctuation on the other interconnect. The induced noise voltage $v_{noise}$ is roughly expressed as $v_{noise} \propto RC_C \cdot dV/dt$, where $C_C$ is a coupling capacitance between two interconnects, and $R$ is resistance between the noise observation point and the ideal voltage source including interconnect resistance and driver resistance. Improvement of transistor performance by process advancement increases $dV/dt$, which results in deterioration of capacitive crosstalk noise. In the case of the equivalent circuit of Fig. 1, the peak voltage of capacitive crosstalk noise $v_{max}$ is approximately expressed by Eq. (1) [12].

$$v_{max} = \frac{RC_C \cdot v_{dd}}{R(C + C_C) + t_r/2},\tag{1}$$

where, $t_r$ is the signal rise time at the aggressor. Equation (1) shows that the noise peak voltage becomes large, but not drastically with respect to $dV/dt$ (=$v_{dd}/t_r$) increase. Reduced interconnect spacing and enlarged aspect ratio of interconnects with technology advance increase coupling capacitance. These qualitative arguments indicate that capacitive crosstalk noise will be severer in the future.

Inductive crosstalk comes from a mutual inductance between interconnects. Assuming two coupled symmetric interconnects, current variation on one interconnect causes a voltage fluctuation on the other interconnect, which is explained with an equation $v_{noise} = M \cdot dI/dt$. $M$ denotes
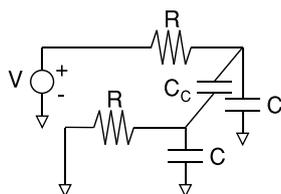
mutual inductance. Higher signal frequency due to technology progress, that is larger $dI/dt$, makes the effect of inductive crosstalk significant. On the other hand, interconnect scaling increases interconnect resistance and characteristic impedance of the interconnect. Large characteristic impedance decreases current flowing in the interconnect and mitigates the effect of inductive crosstalk. Inductive coupling is hardly shielded by signal lines and spreads to wide area, which is different from capacitive coupling. Inductive crosstalk noise is caused by many aggressors, and their noises are superposed, though capacitive crosstalk noise is caused by only adjacent interconnects.

Figure 2 shows an example of noise waveform in the case that capacitive and inductive crosstalk noises simultaneously appear. Supposing two lossless coupled transmission lines, the propagating voltage wave is represented as the sum of even and odd mode waves [2]. The times of flight for capacitive and inductive coupling are given by the Eqs. (2) and (3) respectively.

$$\begin{aligned} t_{Ceven} &= l \sqrt{CL} \\ t_{Codd} &= l \sqrt{(C + 2C_C)L} \end{aligned} \tag{2}$$

$$\begin{aligned} t_{Meven} &= l \sqrt{C(L + M)} \\ t_{Modd} &= l \sqrt{C(L - M)} \end{aligned} \tag{3}$$

where $l$ is interconnect length and $L$ is self inductance of the interconnect. The odd mode wave of inductive coupling travels faster than the other waves and inductive crosstalk appears first as depicted in Fig. 3. Capacitive and inductive crosstalk noises are opposite in voltage to each other, and they somewhat cancel each other, which results in the waveform that a capacitive crosstalk nose follows an inductive crosstalk noise as shown in Fig. 2. In this paper, we call the noise waveform where capacitive crosstalk is dominant as "capacitive crosstalk noise," and the noise wave-
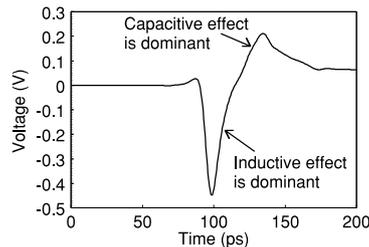


**Fig. 2** An example of crosstalk noise waveform.
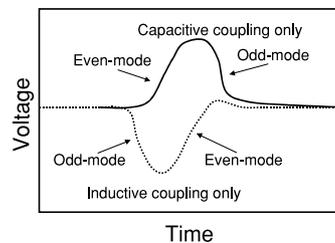


**Fig. 3** Conceptual crosstalk noise waveform considering either only capacitive coupling or only inductive coupling.



**Fig. 1** Equivalent circuit of two symmetric coupled interconnects.

form where inductive crosstalk is dominant as "inductive crosstalk noise," as labeled in Fig. 2.

## 3. Scenarios of Process Advance and Simulation Setup

This paper predicts influence of capacitive and inductive crosstalk based on circuit simulation. In this section, we show two scenarios of process scaling. Simulation setup, which includes interconnect structure, is also described.

### 3.1 Assumed Scenarios

We assume the following two scenarios of process advancement for 90 nm, 65 nm, 45 nm, and 32 nm processes.

**Scenario 1**

    Interconnect cross-section, transistor performance, supply voltage, and dielectric constant of insulator follow ITRS [7], [8] prediction.

**Scenario 2**

    Interconnect cross-section is unchanged, whereas transistor performance, supply voltage, and dielectric constant of insulator follow ITRS [7], [8] prediction similar to Scenario 1.

    In Scenario 1, we assume that the process parameters scale down following ITRS roadmap, which is an industrial standard prediction about the progress of the semiconductor technology.

    Scenario 2 assumes that a thick metal layer is provided for high-speed interconnection and power distribution. We therefore keep the wire cross-section unchanged.

    Interconnect scaling makes interconnect resistance larger because of narrowing interconnect. Larger resistance leads to longer propagation delay of interconnects, which is a disadvantage for high-performance and long-distance signaling. The assumption of interconnect scaling in Scenario 2 means that an interconnect layer, whose size does not scales down and resistance is low are prepared for long-distance signaling. It is reasonable to suppose that interconnect layers with no scaling or slower scaling than ITRS prediction are provided.

### 3.2 Simulation Setup in Scenario 1

In Scenario 1, characteristics of transistor, supply voltage, and dielectric constant come from ITRS prediction. Cross-section of interconnects is scaled down with the ratio described in ITRS roadmap. Table 1 summarizes the parameters at each technology node in Scenario 1.

    The interconnect structure used for crosstalk noise evaluation is shown in Fig. 4. There are eight aggressors and a victim at M6 layer. The victim is placed at the center of aggressors, and power lines locate at both outer sides. In this structure, long-range effect, which is a characteristic unique to inductive coupling, can be evaluated.

    On a real chip, inductive coupling with parallel wires at

**Table 1**   Process parameters in Scenario 1.
'/' separates the parameters of S=W / S=4 W.

| Process | 90 nm | 65 nm | 45 nm | 32 nm |
|---|---|---|---|---|
| Signal rise time(ps) | 25.0 | 15.6 | 10.0 | 6.3 |
| Supply voltage(V) | 1.2 | 1.1 | 1.0 | 0.9 |
| Relative dielectric const. | 3.3 | 2.8 | 2.6 | 2.2 |
| Interconnect width($\mu$m) | 1.00 | 0.67 | 0.49 | 0.35 |
| Interconnect spacing ($\mu$m) | 1.00/4.00 | 0.67/2.68 | 0.49/1.96 | 0.35/1.39 |
| Interconnect thickness ($\mu$m) | 0.90 | 0.64 | 0.49 | 0.34 |
| Num. of division | 9/9 | 14/13 | 21/19 | 35/30 |
| Characteristic impedance | 121/138 | 139/168 | 149/180 | 180/214 |
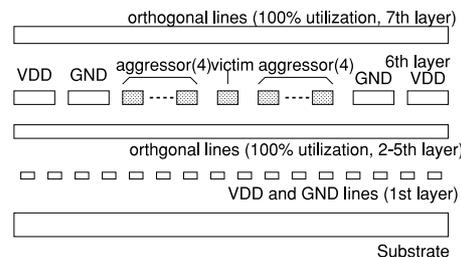


**Fig. 4**   Interconnect structure for RLC extraction and circuit simulation.

other layers also could be a design issue. This paper only examines the bus structure in which all signal lines are aligned at a single layer, however, a similar prediction can be performed straightforward.

    Orthogonal lines are placed at M2-M5, and M7 layers, and their track utilization ratio is 100%. Power/ground lines at M1 layer run parallel to the bus interconnects. Width and thickness of the bus interconnects are set to $1\,\mu$m and $0.9\,\mu$m respectively, and scale in proportion to ITRS prediction at 65–32 nm processes. The $1\,\mu$m-wide interconnects in a 90 nm technology correspond to high performance interconnects. As for wire spacing, we use two parameters; S=W and S=4 W, where W is interconnect width and S is spacing. In S=W structure, wires are placed densely and capacitive crosstalk noise is significant. On the other hand, in S=4 W structure, the spacing is widened so that capacitive crosstalk is suppressed, which is a common technique in current designs. As a result, inductive crosstalk may dominate capacitive crosstalk. The interconnects are 10 mm-long and divided with repeaters. We calculate the number of division using Eq. (4) [13]. Equation (4) gives the division number which makes the propagation delay minimum.

$$k = \sqrt{\frac{0.4 R_{int} C_{int}}{0.7 R_0 C_0}}, \tag{4}$$

where $k$ is the number of division, $R_{int}, C_{int}$ are total resistance and capacitance of the interconnect, $R_0, C_0$ are resistance and capacitance of the minimum size inverter in each process.

    RLC coupled ladder model is adopted as an interconnect model for circuit simulation. Resistance, capacitance, and inductance of interconnects are extracted with a 3D field solver [14]. Orthogonal lines at upper and lower layers and the substrate are considered in capacitance extraction. Return current is assumed to flow only in parallel

power/ground lines at M6 and M1 layers in inductance and resistance extraction. Resistance and inductance of interconnects are frequency dependent, and values at significant frequency [11] are chosen. Significant frequencies of 90 nm, 65 nm, 45 nm, and 32 nm processes are 13.6 GHz, 21.8 GHz, 34 GHz, and 54 GHz respectively. Drivers of interconnects are CMOS inverters, and the size is chosen such that the driver output resistance matches with the characteristic impedance of the interconnect as listed in Table 1. Resistance is often ignored in characteristic impedance calculation especially in the case of high frequency. However, resistance term is not negligible for this evaluation, and we then calculate the characteristic impeda̅ince considering resistance. When evaluating noise peak voltage, the driver is modeled as a resistance for simplicity. Rise signals are input to all aggressors at the same timing and the peak voltage of the victim far-end noise is observed. In propagation delay evaluation, rise signals are input to all aggressors and the victim. We change the relative transition timing between the aggressors and the victim, whereas all aggressors make transitions at the same timing.

We use a transistor model for circuit simulation developed so that DC and AC characteristics match with ITRS2004 prediction [15]. Fundamental parameters such as threshold voltage, on-current, input capacitance and gate delay, are consistent with ITRS prediction. Layout parameters of standard cells of a 90 nm CMOS technology are shrunk for other technologies according to gate length.

### 3.3 Simulation Setup in Scenario 2

In Scenario 2, transistor performance, supply voltage, dielectric constant of insulator are the same with those in Scenario 1. Interconnect width and thickness are set to 1 $\mu$m and 0.9 $\mu$m, and spacing is 1 or 4 $\mu$m at all technology nodes based on the assumption that a high-performance thick interconnect layer will be provided in every technology. Interconnects are 1 mm-long and not divided because the interconnect structure is unchanged. Other conditions on interconnects, such as interconnect layer and bus structure, in Scenario 2 are the same as those in Scenario 1.

## 4. Prediction Results and Discussion

In this section, the impact of capacitive and inductive crosstalk noise at the future technology nodes is estimated based on the assumed scenarios of process advancement explained in Sect. 3.

### 4.1 Scenario 1

Figure 5 shows noise peak voltage normalized by supply voltage in Scenario 1. As process advances, the normalized peak voltage of capacitive crosstalk increases, and that of inductive crosstalk decreases. Shrinking interconnect spacing due to scaling enlarges coupling capacitance between
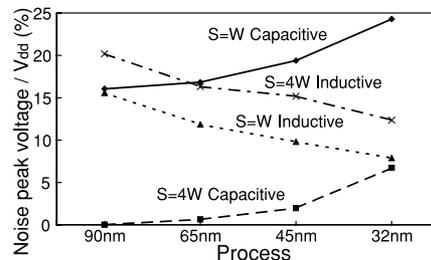


**Fig. 5** Noise peak voltage normalized by $V_{dd}$ in Scenario 1.
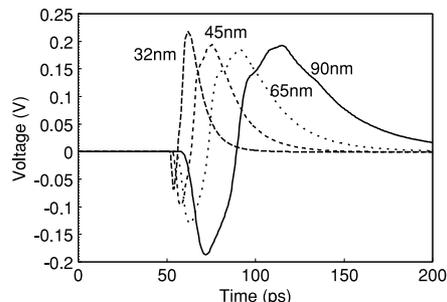


**Fig. 6** Far-end noise waveform in Scenario 1, S=W structure.
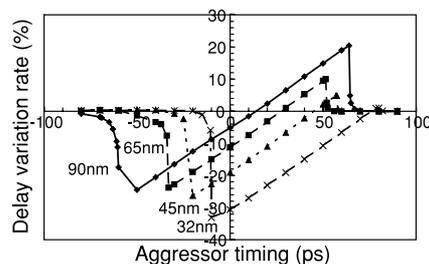


**Fig. 7** Delay variation rate in Scenario 1, S=W structure.

interconnects relatively compared with grounded capacitance, which makes capacitive crosstalk significant. On the other hand, narrowing interconnect increases characteristic impedance of interconnects and decreases current, which results in reduction of inductive crosstalk noise. The high wire resistance also damps inductive noise.

Figure 6 shows the far-end noise waveforms in S=W structure. A gentle concave bump is caused by capacitive crosstalk and a sharp convex spike comes from inductive coupling. In the 90 nm process, both capacitive and inductive crosstalk noises appear. On the other hand, in more advanced processes, capacitive crosstalk becomes dominant in S=W structure and comparable to inductive coupling in S=4 W structure.

Figures 7 and 8 present delay variation rate in Scenario 1. Delay variation rate is defined as $D_{var}/D_{silent}$, where $D_{var}$ is the delay variation and $D_{silent}$ is the delay when all aggressors are silent, i.e. no transitions at aggressors. The delay between 50% points of driver input and final receiver output is observed. In the current configuration of transition direction, delay increase is caused by inductive crosstalk noise, and capacitive crosstalk noise decreases the delay, be-
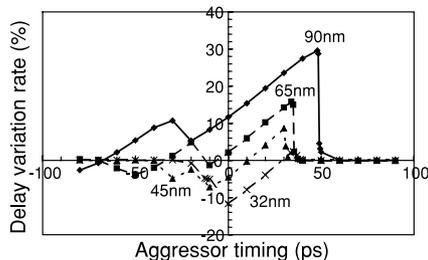
**Fig. 8** Delay variation rate in Scenario 1, S=4 W structure.



**Fig. 9** Noise peak voltage normalized by $V_{dd}$ in Scenario 2.



**Fig. 10** Noise peak voltage of capacitive crosstalk normalized by $V_{dd}$ in Scenario 2.

cause a noise waveform such as Fig. 6 is superposed on the rise transition of the victim. In S=W structure, the impact of capacitive crosstalk dominates that of inductive crosstalk as process advances. Inductive crosstalk is notably suppressed by technology progress even in S=4 W structure. Delay increase due to inductive coupling noise is hardly found in 32 nm technology. We therefore conclude that inductive coupling will be less important in the future advanced technologies.

### 4.2 Scenario 2

Noise peak voltages normalized by supply voltage in Scenario 2 are shown in Fig. 9. The figure indicates that technology progress considerably increases the normalized peak voltage of inductive crosstalk noise because of faster switching speed in advanced processes and the non-scaled interconnect structure in Scenario 2. On the other hand, the effect of capacitive crosstalk is slightly reduced.

Figure 10 compares the normalized peak voltages of capacitive crosstalk noise simulated with RLC ladder model and with RC ladder model. The effect of capacitive crosstalk



**Fig. 11** Delay variation rate in Scenario 2, S=W structure.



**Fig. 12** Delay variation rate in Scenario 2, S=4 W structure.

simulated with RC model increases as seen in Fig. 10, which is consistent with the relation between capacitive crosstalk and rise time of aggressor signal [12], [16]. Figure 10 implies that capacitive crosstalk noise is overwhelmed by inductive noise because consideration of inductance mitigates capacitive crosstalk.

Figures 11 and 12 present delay variation rate in Scenario 2. The impact of inductive crosstalk, which is observed as positive delay variation, is dominative. Though there is considerable increase of noise peak voltage in Fig. 9, the maximum delay variation is scarcely deteriorated. Increase of noise peak voltage is not tightly reflected in the delay variation. This is because the delay variation due to inductive crosstalk noise depends on both the noise peak voltage and the noise width.

As far as either capacitive or inductive crosstalk extremely dominates the other, the period in which inductive crosstalk noise appears mainly depends on the difference between the times of flight for capacitive and inductive coupling as depicted in Figs. 2 and 3. A longer interconnect enlarges the difference of the times of flight, and delay variation due to inductive crosstalk noise increases as shown in Fig. 13.

The timing range, when inductive crosstalk effect is dominant, becomes narrower in advanced processes. Figure 14 presents the detail of Fig. 12 concerning aggressor timing from −10 to 20 ps. Inductive crosstalk effect on timing appears when inductive crosstalk noise overlaps signal transition waveform. Advancement of MOS performance shrinks signal rise time, and the overlappable timing range decreases, which results in the narrower timing range in Fig. 14.

We find the second peak of positive delay variation near −20 to −30 aggressor timing in Figs. 8, 11, 12. Figure 15

**Fig. 13** Maximum interconnect delay variation vs. interconnect length.



**Fig. 14** The detail of Fig. 12 concerning aggressor timing from −10 to 20 ps.



**Fig. 15** Far-end noise waveform in 32 nm process, S=4 W structure.



**Fig. 16** Wire structure for determining aspect ratio.

servation motivates us to explore the tradeoff between the worst-case delay considering inductive coupling noise and interconnect cross-sectional area. We here examine whether there is a wire cross-section that makes inductive coupling ignorable with a small penalty of delay increase. In other words, we evaluate the maximum performance of interconnects whose inductive coupling does not have a significant impact on timing design.

## 5.1 Evaluation Setup

We evaluate the interconnect propagation delay varying cross-sectional area from $1\,\mu m^2$ to $0.05\,\mu m^2$. The interconnect structure for RLC extraction and evaluation conditions are the same as Scenario 1 in Sect. 3. S=4 W structure is evaluated because we focus on the effect of inductive crosstalk. Drivers of aggressors and victim are 32X inverters.

The aspect ratio of interconnect at each cross-sectional area and process is decided such that the worst-case delay considering capacitive crosstalk is minimized.

You might think that circuit designers could not change the interconnect thickness. However, we think that the integration of inductive crosstalk free interconnect is one of the design strategies co-operated by circuit designers and process integrators, and we hence determine the aspect ratio for each process and cross-sectional area. The worst-case delay is estimated by circuit simulation with an interconnect structure in Fig. 16.

Generally, most of interconnects are routed with S=W, and the coupling capacitance is large. We therefore minimizes the worst-case delay of capacitive crosstalk noise as an metric in this paper.

Resistance and capacitance of interconnects are calculated from formulas in [17], [18]. In deriving the aspect ratio, the coupling capacitance is doubled for considering Miller effect of capacitive coupling for simplicity. From these consideration, the aspect ratios are set to 1.4–1.7.

## 5.2 Experimental Results and Discussion

Figure 17 plots the relation between the worst-case delay and delay variation rate with 90 nm and 32 nm transistor models. In Fig. 17, points with larger worst-case delay and smaller delay variation correspond to smaller cross-sectional area. The worst-case delay is larger in narrower interconnects even if inductive crosstalk is considered. On the other hand, starting from the smaller worst-case value,

shows the far-end noise waveform in 32 nm process, S=4 W structure, as an example. There are two convex peaks in the waveform. The second peak of delay variation derives from the second peak of the convex waveform. The second convex peak caused by the difference of the time of flight among even and odd mode of capacitive and inductive coupling.

## 5. Wire Cross-Sectional Area Tuning for Inductive Crosstalk Free Interconnects

Thick and wide interconnects generally provide short propagation delay, yet consumes large interconnect resource. Our prediction in Sect. 4 demonstrates that thick and wide interconnects in Scenario 2 involve larger inductive crosstalk, which may mean that interconnect delay will not be nicely improved even with thick and wide interconnects in the future if special techniques such as differential signaling and shield insertion are not used. On the other hand, narrowing interconnect reduces delay uncertainty due to inductive crosstalk, because it increases wire resistance. However, unfortunately propagation delay also increases. This ob-

**Fig. 17** The worst-case delay vs. delay variation rate when cross-sectional are is varied.
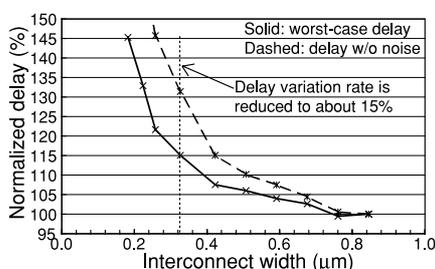


**Fig. 18** Normalized delay vs. interconnect width. Absolute delay values of worst-case delay and delay without noise at $1\,\mu m^2$ area are 160 and 120 ps respectively.

i.e. large cross-sectional area, up to a certain point, narrowing interconnect notably reduces delay variation rate despite small degradation of the worst-case delay.

Figure 18 presents delay vs. interconnect width, where delay w/o noise is the delay without crosstalk noises, and the worst-case delay means the delay degraded with the maximum delay variation due to inductive crosstalk noise. The delay shown in Fig. 18 is normalized by the delay with $1\,\mu m^2$ cross-sectional area. Please note that shrinking wire cross-section narrows interconnect width, and saves the interconnect resource.

Suppose here that the influence of inductive coupling can be ignored if the delay variation rate is smaller than 15%. The delay variation rate at $0.16\,\mu m^2$ area is about 15% in 32 nm process from Fig. 17. Compared with $1\,\mu$m-wide interconnects, the use of interconnect resource is reduced by 61%. When the crosstalk noise is not considered, shrinking interconnect degrades the delay by 31% in Fig. 18. However, as a matter of fact, the worst-case delay considering inductive crosstalk noise increases only by 15%. This result indicates that narrowing cross-sectional area of high-performance interconnects can improve both interconnect efficiency and delay variation due to inductive coupling in spite of small deterioration of the interconnect propagation delay. In addition, narrowed wires make special design effort to care for inductive coupling unnecessary.

## 6. Conclusion

In this paper, we have presented the prediction of capacitive and inductive crosstalk effect in prospective processes. The peak noise voltage and delay variation due to crosstalk noise

are evaluated in two scenarios, where interconnects scale down and do not scale. In the scenario with scaling, capacitive coupling will be more dominant and inductive coupling will be less important as technology advances. On the other hand, in the scenario without interconnect scaling, inductive coupling will be dominant.

The evaluation of the tradeoff between wire cross-sectional area and propagation delay considering inductive coupling noise is also presented. Shrinking the interconnect cross-section increases the propagation delay, but its increasing ratio is much reduced because higher wire resistance mitigates inductive coupling noise. An appropriate selection of interconnect cross-sectional area makes consideration of inductive coupling unnecessary with the small sacrifice of propagation delay.

**References**

[1] D. Sylvester and K. Keutzer, "Getting to the bottom of deep submicron," Proc. ICCAD, pp.203–211, Nov. 1998.

[2] K. Agarwal, D. Sylvester, and D. Blaauw, "A simplified transmission-line based crosstalk noise model for on-chip RLC wiring," Proc. ASP-DAC, pp.858–864, Jan. 2004.

[3] Y. Massoud, J. Kawa, D. Macmillen, and J. White, "Modeling and analysis of differential signaling for minimizing inductive crosstalk," Proc. DAC, pp.804–809, June 2001.

[4] T. Sato, D. Sylvester, Y. Cao, and C. Hu, "Accurate in-situ measurement of noise peak and delay induced by interconnect coupling," IEEE J. Solid-State Circuits, vol.36, no.10, pp.1587–1591, Oct. 2001.

[5] A. Deutsch, et al., "Modeling and characterization of long on-chip interconnections for high-performance microprocessors," IBM J. Res. Dev., vol.39, no.5, pp.547–567, 1995.

[6] Y. Ogasahara, M. Hashimoto, and T. Onoye, "Measurement of inductive coupling effect on timing in 90 nm global interconnects," Proc. CICC, pp.721–724, Sept. 2006.

[7] International Technology Roadmap for Semiconductors, "International technology roadmap for semiconductors 2004 update process integration, devices, and structures," 2005.

[8] International Technology Roadmap for Semiconductors, "International technology roadmap for semiconductors 2004 update interconnect," 2005.

[9] A. Sakai, T. Yamada, Y. Matsushita, and H. Yasuura, "Reduction of coupling effects by optimizing the 3-D configuration of the routing grid," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol.11, no.5, pp.951–954, Oct. 2003.

[10] R. Kumar, "Interconnect and noise immunity design for the Pentium 4 processor," Proc. DAC, pp.938–943, June 2003.

[11] C. Cheng, J. Lillis, S. Lin, and N.H. Chang, Interconnect analysis and synthesis, Wiley-Interscience Publication, 2000.

[12] J. Cong, D.Z. Pan, and P.V. Srinivas, "Improved crosstalk modeling for noise constrained interconnect optimization," Proc. ASP-DAC, pp.373–377, Jan. 2001.

[13] H.B. Bakoglu, Circuits, interconnections, and packaging for VLSI, Addison-Wesley Publication, 1990.

[14] Synopsys Corp., "Raphael interconnect analysis program reference manual," June 2004.

[15] http://www-lab13.kuee.kyoto-u.ac.jp/~tsuchiya/tr-model.html.en

[16] J.M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital integrated circuits a design perspecitve, Pearson Education, 2003.

[17] http://www.eecs.umich.edu/~dennis/bacpac/index.html

[18] J.H. Chern, J. Huang, L. Arledge, P.C. Li, and P. Yang, "Multilevel metal capacitance models for CAD design synthesis systems," IEEE Electron Device Lett., vol.13, pp.32–34, Jan. 1992.

**Yasuhiro Ogasahara** received B.E. degree in Electronic Engineering and M.E. in Information Systems Engineering from Osaka University in 2003 and 2005, respectively. He is currently a doctor course student of Graduate School of Information Science and Technology, Osaka University. His research interests are signal integrity and power integrity. He is a student menber of IEEE.

**Masanori Hashimoto** received the B.E., M.E. and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively. Since 2001, he was an Instructor in Department of Communications and Computer Engineering, Kyoto University. Since 2004, he has been an Associate Professor in Department of Information Systems Engineering, Graduate School of Information Science and Technology, Osaka University. His research interest includes computer-aided-design for digital integrated circuits, and high-speed circuit design. Dr. Hashimoto served on the technical program committees for international conferences including DAC, ICCAD, ASP-DAC, ICCD and ISQED. He is a member of IEEE, ACM and IPSJ.

**Takao Onoye** received B.E. and M.E. degrees in Electronic Engineering, and Dr. Eng. degree in Information Systems Engineering all from Osaka University, Japan, in 1991, 1993, and 1997, respectively. He is currently a professor in the Department of Information Systems Engineering, Osaka University. His research interests include media-centric low-power architecture and its SoC implementation. He is a member of IEEE, IPSJ, and ITE-J.